MCP Specification

2Gb (128Mb x16) NAND Flash
+ 1Gb (64Mb x16) mobile DDR

Document Title

MCP
2Gb (128Mb x16) NAND Flash / 1Gb (64Mb x16) DDR

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft - 2Gb NAND Flash B-Die - 1Gb mobile DDR A-Die	May 2009	Preliminary
0.2	Update - tXP Note19	May 2009	Preliminary
1.0	Final Version	Aug. 2009	

FEATURES

[MCP]

- Operation Temperature
  - -30°C ~ 85°C
- Packcage
  - 149-ball FBGA - 10.0x14.0mm^2, 1.2t, 0.8mm pitch
  - Lead & Halogen Free

[NAND Flash]

- Multiplane Architecture
- Supply Voltage
  - Vcc = 1.7 - 1.95 V
- Memory Cell Array
  - (1K + 32) words x 64 pages x 2048 blocks
- Page Size
  - (1K+ 32 spare) Words
- Block Size
  - (64K + 2K spare) Words
- Page Read / Program
  - Random access : 25us (max.)
  - Sequential access : 45ns (min.)
  - Page program time : 250us (typ.)
  - Multi-page program time (2 pages) : 250us (typ.)
- COPY BACK PROGRAM
  - Automatic block download without latency time
- FAST BLOCK ERASE
  - Block erase time: 2.0ms (typ.)
  - Multi-block erase time (2 blocks) : 2.0ms (typ.)
- CACHE READ
  - Internal (2048 + 64) Byte buffer to improve the read throughtput.
- STATUS REGISTER
  - Normal Status Register (Read/Program/Erase)
  - Extended Status Register (EDC)
- BLOCK PROTECTION
  - To Protect Block against Write/Erase
- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions.
- DATA RETENTION
  - 100,000 Program/Erase cycles (with 1bit/528byte ECC)
  - 10 years Data Retention

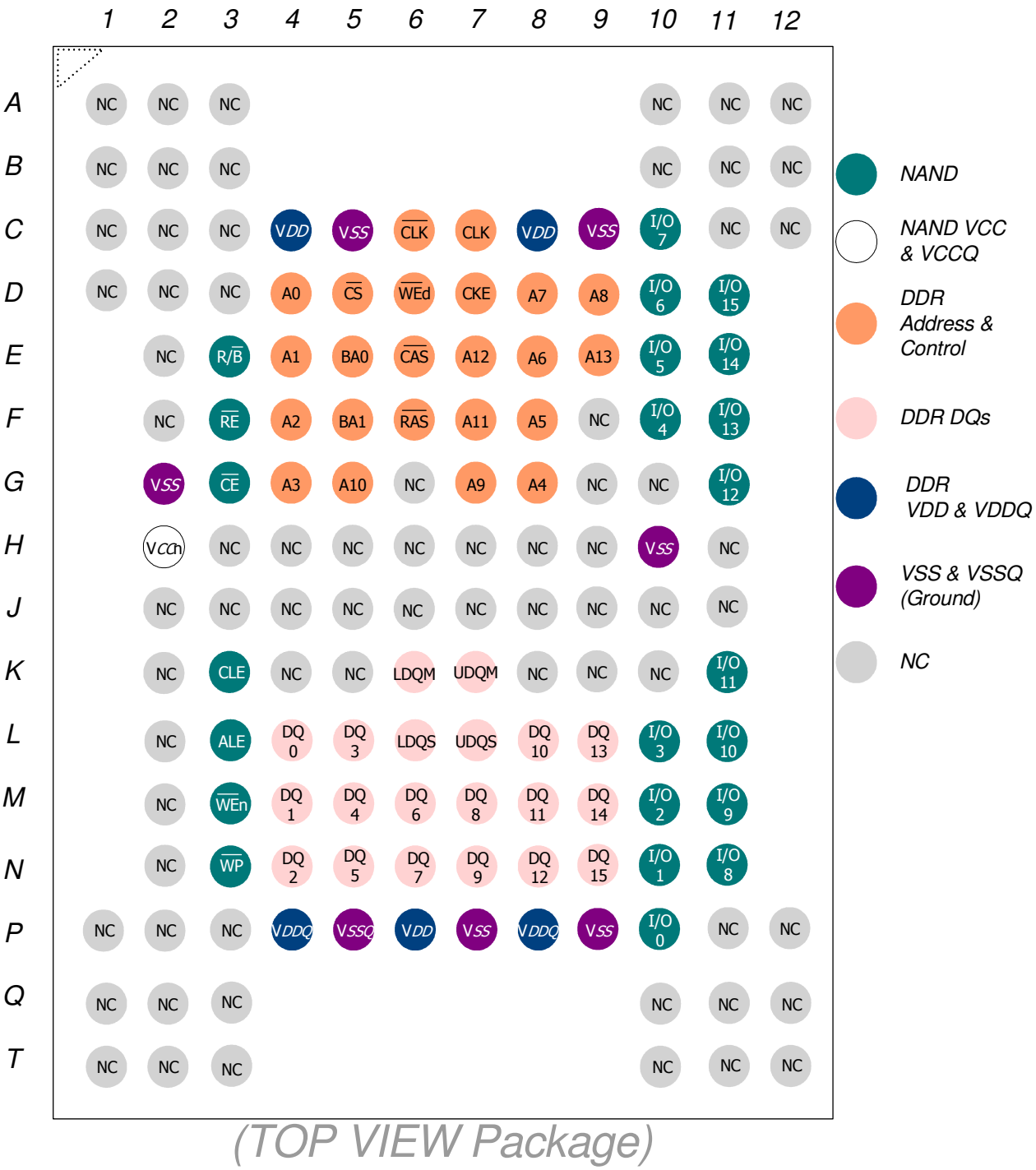
[DDR SDRAM]

- Double Data Rate architecture
  - two data transfer per clock cycle
- x16 bus width
- Supply Voltage
  - VDD / VDDQ = 1.7 - 1.95 V
- Memory Cell Array
  - 16Mb x 4Bank x 16 I/O
- Bidirectional data strobe (DQS)
- Input data mask signal (DM)
- Input Clock
  - Differential Clock Inputs (CK, /CK)
- MRS, EMRS
  - JEDEC Standard guaranteed
- CAS Latency
  - Programmable CAS latency 2 or 3 supported
- Burst Length
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H8BCS0SI0BAR-46M	NAND Flash mobile DDR	1.8V 1.8V	2Gb (128Mb x16) 1Gb (64Mb x16)	45ns DDR333	149Ball FBGA (Lead & Halogen Free)
H8BCS0SI0BAR-4EM	NAND Flash mobile DDR	1.8V 1.8V	2Gb (128Mb x16) 1Gb (64Mb x16)	45ns DDR400	149Ball FBGA (Lead & Halogen Free)

149Ball ASSIGNMENT



(TOP VIEW Package)

Pin Description

SYMBOL	DESCRIPTION

< 2Gb (128Mb x16) NAND Flash >

I/O0 ~ I/O15	Data Input / Output
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy Out
VCC	Supply Voltage
VSS	Ground

< 1Gb (64Mb x16) mobile DDR >

CK, $\overline{CK}$	Differential Clock Inputs
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Command Inputs
BA0, BA1	Bank Address Inputs
A0 ~ A13	Address Inputs
DQ0 ~ DQ15	Data Bus
LDM, UDM	Input Data Mask
LDQS, UDQS	Data Strobe
VDD	Power Supply
VSS	Ground
VDDQ	I/O Power Supply
VSSQ	I/O Ground

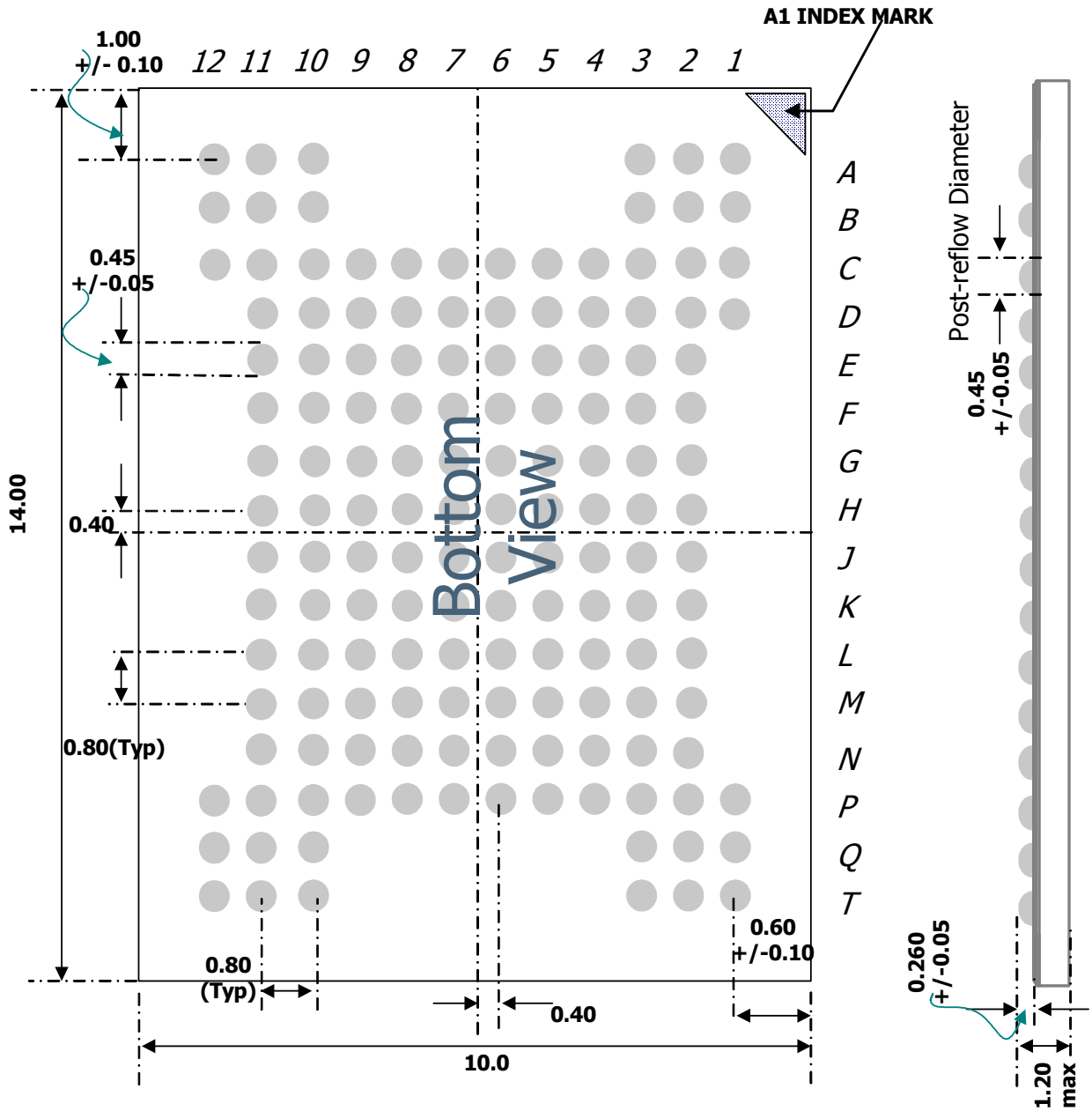
< Common >

DNU	Do Not Use
NC	No Connection

PACKAGE INFORMATION

149 Ball 0.8mm pitch 10.0mm x 14.0mm FBGA *[t = 1.2mm max]*

Unit [mm]



2Gb(128Mbx16) NAND FLASH B-Die

1.SUMMARY DESCRIPTION

The Hynix NAND Flash has 2Gbit with spare 8Mx8 bit capacity. The device is offered in 1.8V Vcc Power Supply, and with x16 I/O interface Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 2048 blocks, composed by 64 pages. A program operation allows to write the 2112-byte page in typical 250us and an erase operation can be performed in typical 2.0ms on a 128K-byte block.

Data in the page can be read out at 45ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input.
This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input. The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management. When a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation: 1bit error out of every 264-word can be detected. Due to this feature, it is no more nor necessary nor recommended to use external 2-bit ECC to detect copy back operation errors. Data read out after copy back read (both for single and multiplane cases) is allowed.

Even the write-intensive systems can take advantage of the Hynix NAND Flash extended reliability of 100K program/ erase cycles by supporting ECC (Error Correcting Code) with real time mapping-out algorithm. The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.
This device includes also extra features like OTP/Unique ID area, Read ID2 extension, and Block Protection.
Especially Block Protection allows protection on Block 0 or OTP area of the device against Write/Erase operations on that block.

1.1 Product List

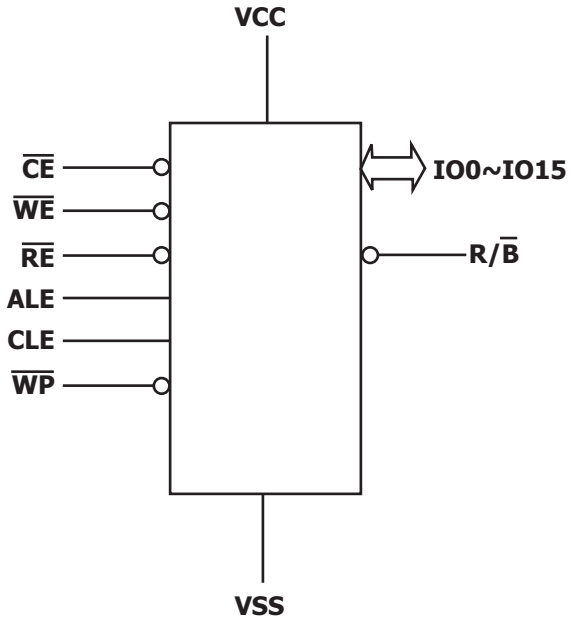


Figure1: Logic Diagram

IO15 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO15(1)	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. For x16 version only
2. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
3. An internal voltage detector disables all functions whenever VCC is below 1.1V (1.8V version) to protect the device from any involuntary program/erase during power transitions.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	I/O8-IO15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L(1)
2nd Cycle	A8	A9	A10	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L(1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	L(1)
5th Cycle	A27	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 4: Address Cycle Map(x16)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ1	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PGM	85h	10h	-	-	
MULTI PLANE PROGRAM	80h	11h	81h	10h	
MULTI PLANE COPYBACK PROGRAM	85h	11h	81h	10h	
BLOCK ERASE	60h	D0h	-	-	
MULTI PLANE BLOCK ERASE	60h	60h	D0h	-	
READ STATUS REGISTER	70h	-	-	-	Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (RANDOM)	00h	31h	-	-	
READ CACHE (SEQUENTIAL)	31h	-	-	-	
READ CACHE END	3Fh	-	-	-	
READ EDC STATUS REGISTER	7Bh	-	-	-	

Table 5: Command Set

Note:
1. READ EDC STATUS REGISTER is only available on Copy Back operation.

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 6: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 3ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be
high. See Figure 4 and Table 13 for details of the timings requirements. Command codes are always applied on IO7:0.

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses
for the 4Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable
low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 13 for details of the timings requirements. Addresses are always applied on IO7:0.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 6 and Table 13 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC
register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 7,8,10,11,12 and Table 13 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modifying operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read

This operation is operated by writing 00h and 30h to the command register along with five address cycles.
Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 1056 words of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 45ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Page Program

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8 times. The addressing should be done on each pages in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The bytes other than those to be programmed do not need to be loaded. The device supports random data input in a page.
The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 details the sequence.

3.3 Multi Plane Program

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<18>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<18>=1). The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/$\overline{B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in 1st or 2nd page program, fail bit of status register will be set: Device supports pass/fail status of each plane. Figure 19 details the sequence.

3.4 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in there cycles initiated by an Erase Setup command (60h). Only address A17 to A27 is valid while A11 to A16 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.
Once the erase process starts, the Read Status Register command may be entered to read the status register.
The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 18 details the sequence.

3.5 Multi Plane Erase

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.
Block erase setup command (60h) must be repeated two times, each time followed by 1st block and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multiplane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion. Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program. Figure 20 details the sequence

3.6 Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register.
When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 16 & Figure 17). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure17.

Copy-back program operation is allowed only within same plane.

3.7 Multi-Plane Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also need to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling $\overline{RE}$ (See Figure 21), or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 21.

Most NAND devices require 2 bit external ECC only due to copy back operation while 1 bit ECC can be enough for all other operation. Reason is that during read for copy back + copy back program sequence a bit error due to charge loss is not checked by external error detection/correction scheme. On the contrary, 2Gbit NAND includes automatic Error Detection Code during copy back operation: thanks to this, 2 bit external ECC is no more required, with significant advantage for customers that can always use single bit ECC. More details on EDC operation are available in section 3.8.

3.8 EDC Operation

Error Detection Code check automatically starts immediately after device becomes busy for a copy back program operation (both single and multiple plane). In the x16 version EDC allows detection of 1 single bit error every 264 words, where each 264 word group is composed by 256 words of main array and 8 words of spare area (see Table 20,21). So described 264 word area is called " EDC unit".

To Properly use EDC, some limitations apply:
- Random data input can be used only once in copy back program or page program or multiple page program, unless user inputs data for a whole EDC unit (or more whole EDC units).
- Any page program operation must be done on whole page basis, or on whole EDC unit.

EDC result can be checked only during copy back program through 7Bh (specific Read EDC register command, Table 22)

3.9 Read Status Register

The device contains a Status Register which may be read to find out whether, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random data output, the read command (00h) should be given before starting read cycles.

3.10 Read EDC Status Register

The operation is available only in copy back program and it allows the detection of errors occurred during read for copy back. In case of multiple plane copy back, it is not possible to know which of the two read operation caused the error. After writing 7Bh command to the command register, a read cycle outputs the content of the EDC Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last.
Operation is same read status register command. Refer to below Table 22 for specific EDC Register definitions.

3.11 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence, while tables 15 explain the byte meaning.

3.12 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin goes low for tRST after the Reset command is written. Refer to Figure 25.

3.13 Cache Read

Cache read can be used to increase the read operation speed when accessing sequential pages within a block. First, issue a normal page read (00-30h). See figure 13.

The R/$\overline{B}$ signal goes low for tR during the time it takes to transfer the first page of data from the memory to the data register. After R/$\overline{B}$ returns to high (31h) command is latched into the command register. R/$\overline{B}$ goes low while data is being transferred from the data register to the cache register. After the data register contents are transferred to the cache register, another page read is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially from the cache register. If the total time to output data exceeds tR, then the page read is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/$\overline{B}$ will stay low. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command.

If the data transfer from memory to the data register is not completed before the 31h command is issued, R/$\overline{B}$ stays low until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/$\overline{B}$ will stay low until the previous page read is complete and the data has been transferred to the cache register.

To read out the last page of data (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another page read.

4. OTHER FEATURES

4.1 Data Protection & Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V(1.8V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 26. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied.

Because pull-up resistor value is related to tR(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Fig 27). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	2008	-	2048	Blocks

Table 7 : Valid Blocks Numbers

NOTE:
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	V
$VIO^{(2)}$	Input or Output Voltage	-0.6 to 2.7	V
Vcc	Supply Voltage	-0.6 to 2.7	V

Table 8: Absolute maximum ratings

NOTE:

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

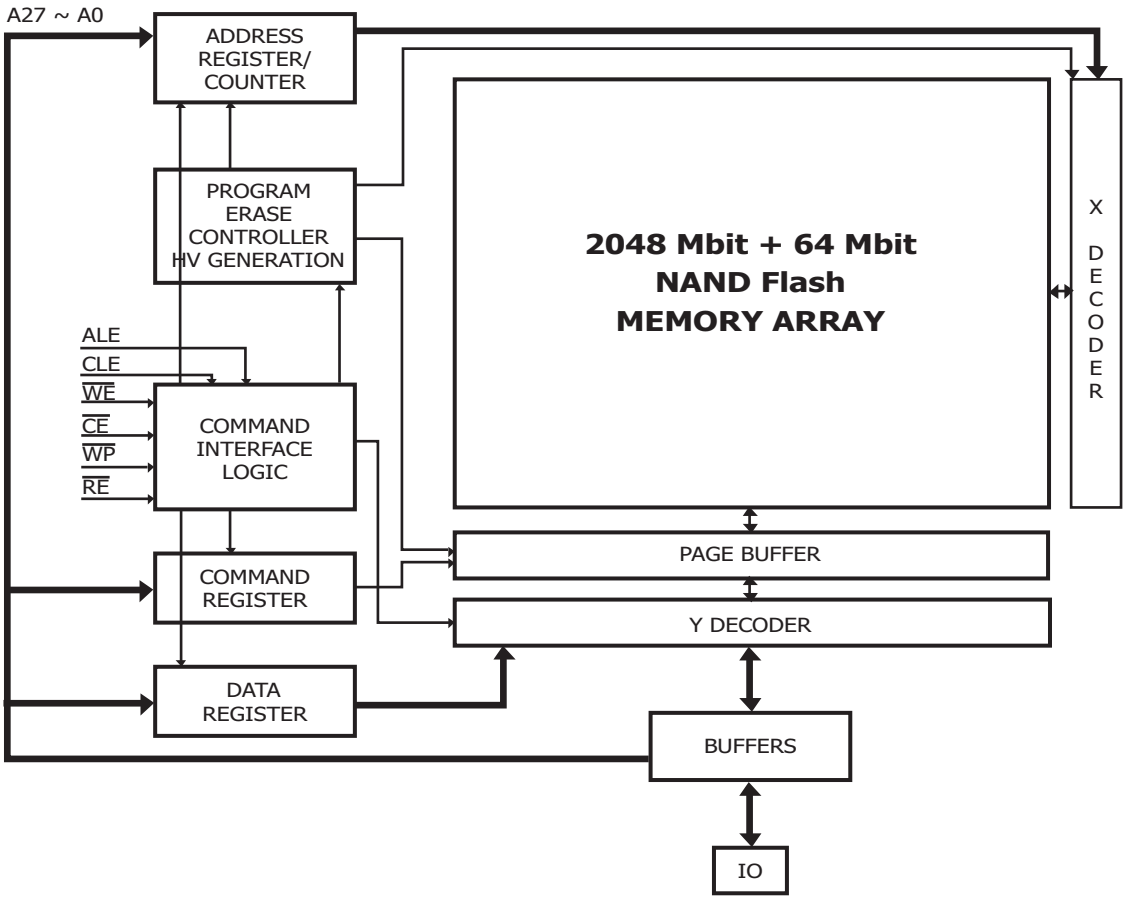


Figure 3: Block Diagram

Parameter		Symbol	Test Conditions	1.8Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC}=45ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Program	I_{CC2}	-	-	10	20	mA
	Erase	I_{CC3}	-	-	10	20	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/Vcc	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	± 10	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to Vcc (max)	-	-	± 10	uA
Input High Voltage		V_{IH}	-	0.8xVcc	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		V_{OH}	I_{OH}=-100uA	Vcc-0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=100uA	-	-	0.1	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}=0.2V	3	4	-	mA

Table 9: DC and Operating Characteristics

Parameter	Value
	1.8Volt
Input Pulse Levels	0V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC/2
Output Load (1.7V - 1.95V)	1 TTL GATE and CL=30pF

Table 10: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Table 11: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time / Multi-Plane Program Time	t_{PROG}	-	250	700	us
Dummy Busy Time for Two Plane Program	t_{DBSY}	-	0.5	1	us
Number of partial Program Cycles in the same page	NOP	-	-	8	Cycles
Block Erase Time / Multi-Plane Block Erase Time	t_{BERS}	-	2	2.5	ms
Read Cache Busy Time	t_{RBSY}	-	3	tR	us

Table 12: Program / Erase Characteristics

Parameter	Symbol	1.8V		Unit
		Min	Max	
CLE Setup time	t_{CLS}	25		ns
CLE Hold time	t_{CLH}	10		ns
$\overline{CE}$ setup time	t_{CS}	35		ns
$\overline{CE}$ hold time	t_{CH}	10		ns
$\overline{WE}$ pulse width	t_{WP}	25		ns
ALE setup time	t_{ALS}	25		ns
ALE hold time	t_{ALH}	10		ns
Data setup time	t_{DS}	20		ns
Data hold time	t_{DH}	10		ns
Write Cycle time	t_{WC}	45		ns
$\overline{WE}$ High hold time	t_{WH}	15		ns
Data Transfer from Cell to register	t_R		25	us
ALE to $\overline{RE}$ Delay	t_{AR}	10		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		ns
Ready to $\overline{RE}$ Low	t_{RR}	25		ns
$\overline{RE}$ Pulse Width	t_{RP}	25		ns
$\overline{WE}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	45		ns
$\overline{RE}$ Access Time	t_{REA}		30	ns
$\overline{RE}$ High to Output High Z	t_{RHZ}		100	ns
$\overline{CE}$ High to Output High Z	t_{CHZ}		50	ns
$\overline{CE}$ High to Output hold	t_{COH}	15		ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5		ns
$\overline{RE}$ High Hold Time	t_{REH}	10		ns
Output High Z to $\overline{RE}$ low	t_{IR}	0		ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10		ns
Address to data loading time	t_{ADL}	100		ns
$\overline{WE}$ High to $\overline{RE}$ low	t_{WHR}	60		ns
$\overline{RE}$ High to $\overline{WE}$ low	t_{RHW}	100		ns
Device Resetting Time (Read / Program / Erase)	t_{RST}		5/10/500(1)	us
Write Protection time	t_{WW}(2)	100		ns

Table 13: AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.

IO	Page Program	Block Erase	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	NA	-
2	NA	NA	NA	NA	-
3	NA	NA	NA	NA	-
4	NA	NA	NA	NA	-
5	Ready / Busy	Ready / Busy	Ready / Busy	Ready/Busy	Busy: '0' Ready:'1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready/Busy	Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	NA	Protected: '0' Not Protected: '1'

Table 14 : Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 15: Device Identifier Coding

Device	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd cycle	4th cycle	5th cycle
NAND Flash	1.8V	x16	ADh	BAh	10h	55h	44h

Table 16: Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave program Between multiple chips	Not Supported		0 1			
Write Cache	Not Supported	0 1				

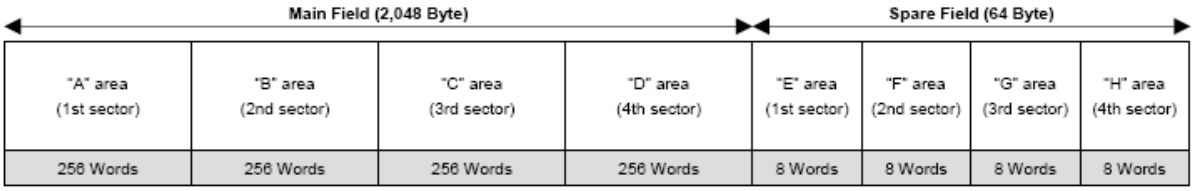
Table 17: 3rd Byte of Device Idendifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	50ns 30ns 25ns Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64K 128K 256K 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 18: 4th Byte of Device Identifier Description

	Description	IO7	IO6 IO5 IO4	IO3 IO2	IO1	IO0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Reserved		0			0	0

Table 19: 5rd Byte of Device Idendifier Description



Sector	Main Field (Column 0~1, 1023)		Spare Field (Column 1,024~1,055)	
	Area Name	Column Address	Area Name	Column Address
1st 264 Words Sector	"A"	0 ~ 255	"E"	1,024 ~ 1,031
2nd 264 Words Sector	"B"	256 ~ 511	"F"	1,032 ~ 1,039
3rd 264 Words Sector	"C"	512 ~ 767	"G"	1,040 ~ 1,047
4th 264 Words Sector	"D"	768 ~ 1,023	"H"	1,048 ~ 1,055

Table 21: Page organization in EDC units (x16)

IO	Copy back Program	CODING
0	Pass/Fail	Pass: '0' Fail: '1'
1	EDC status	NO error: '0'
2	EDC Validity	Invalid: '0' Valid: '1'
3	NA	-
4	NA	-
5	Ready/Busy	Busy: '0' Ready: '1'
6	Ready/Busy	Busy: '0' Ready: '1'
7	Write Protect	Protected: '0' Not Protected: '1'

Table 22: EDC Register Coding

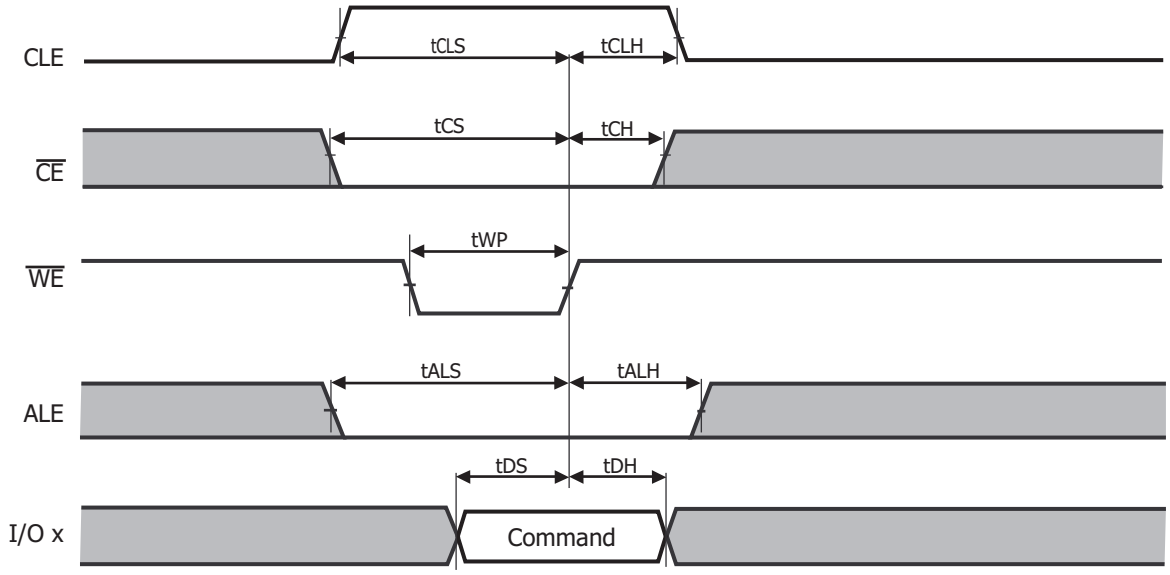


Figure 4: Command Latch Cycle

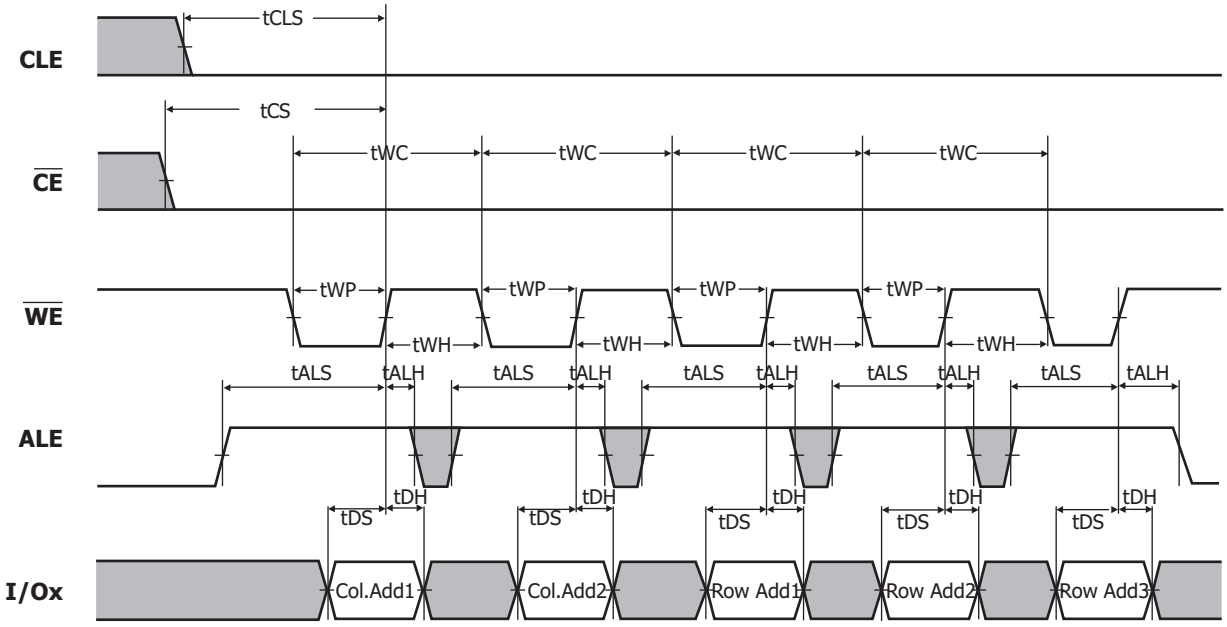
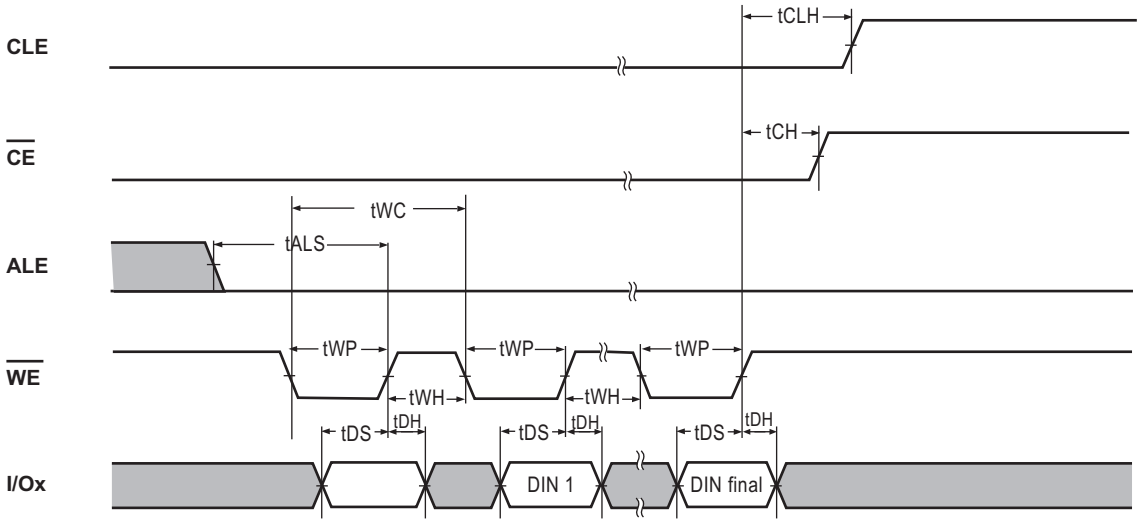
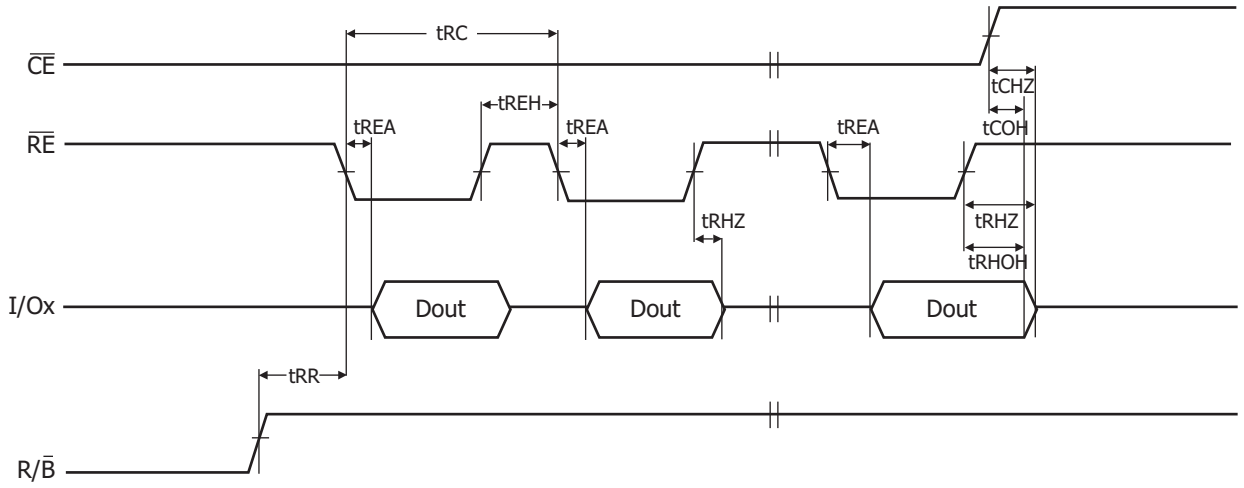


Figure 5: Address Latch Cycle



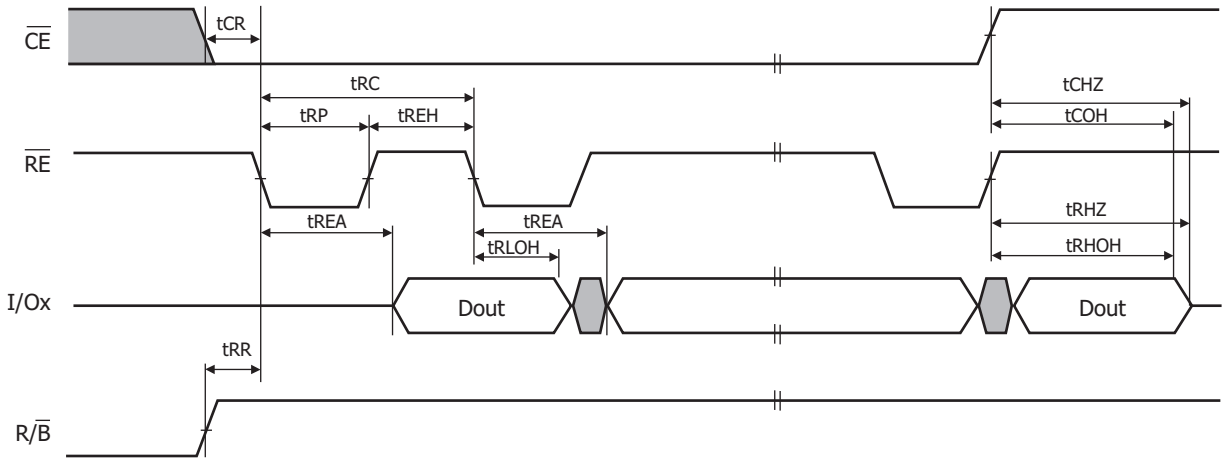
Notes: DIN final means 2,112Bytes (x8)

Figure 6: Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 7: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read (EDO Type CLE=L, $\overline{WE}$=H, ALE=L)

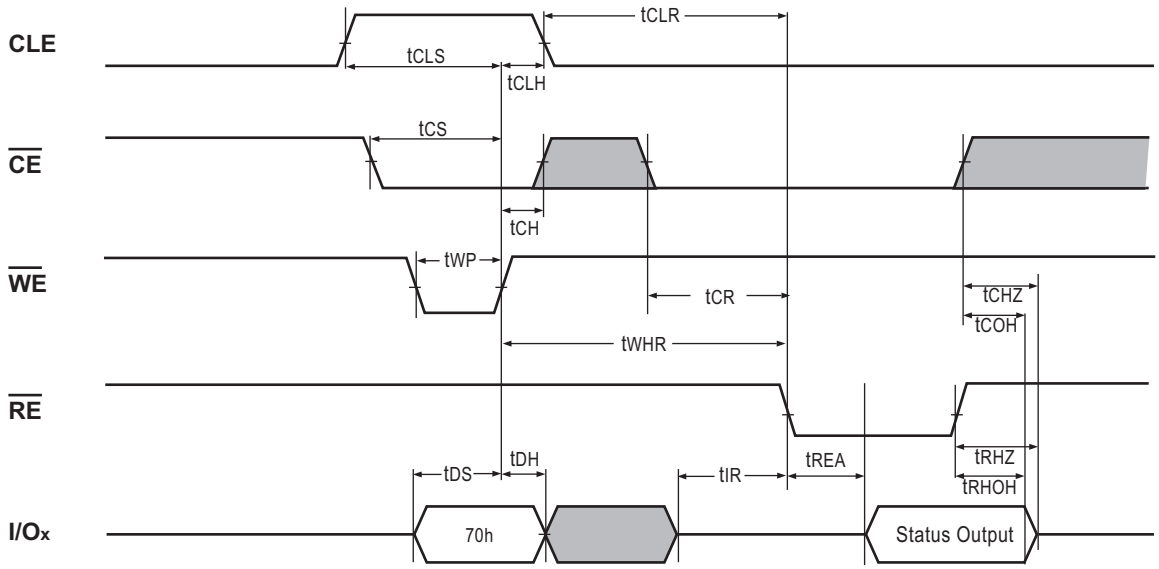


Figure 9: Status Read Cycle

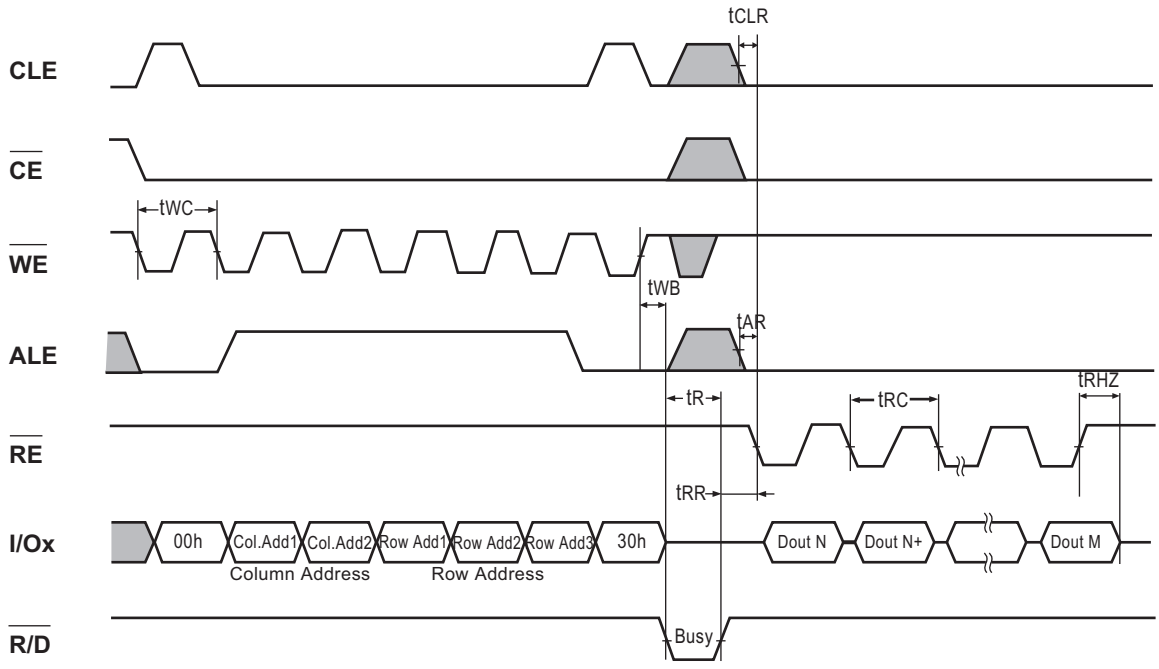


Figure 10: Read1 Operation (Read One Page)

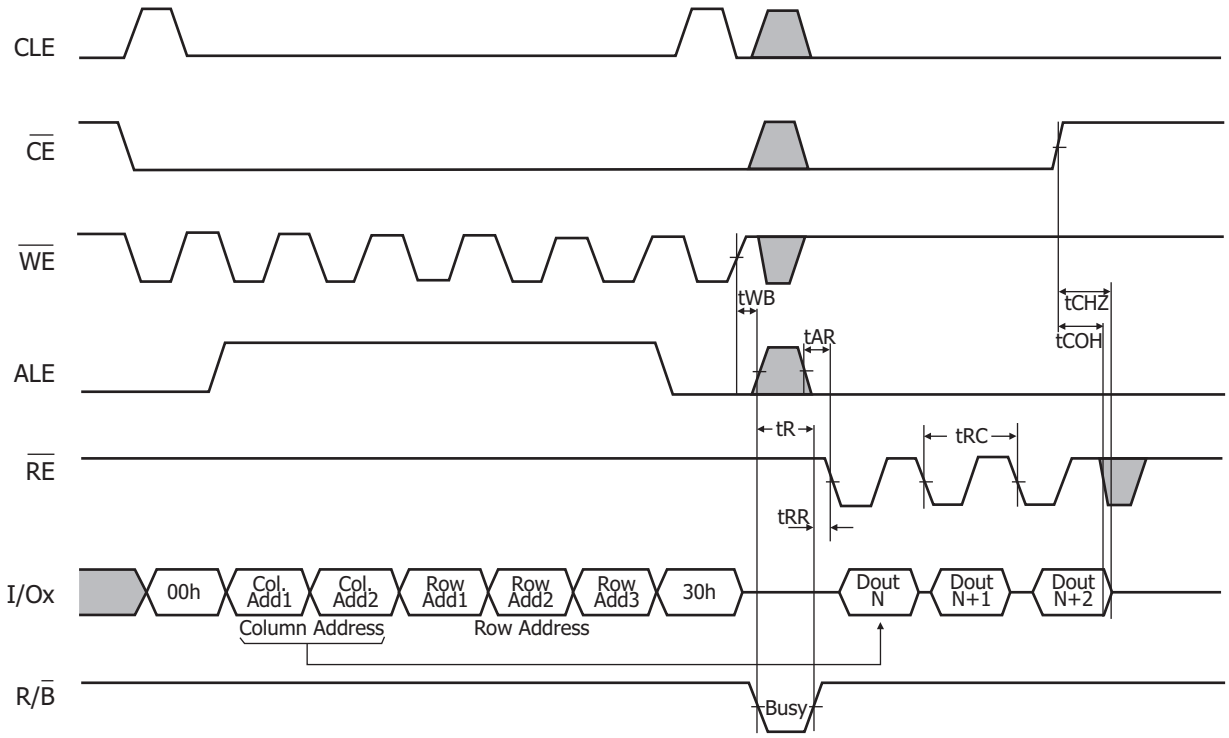


Figure 11: Read1 Operation intercepted by $\overline{CE}$

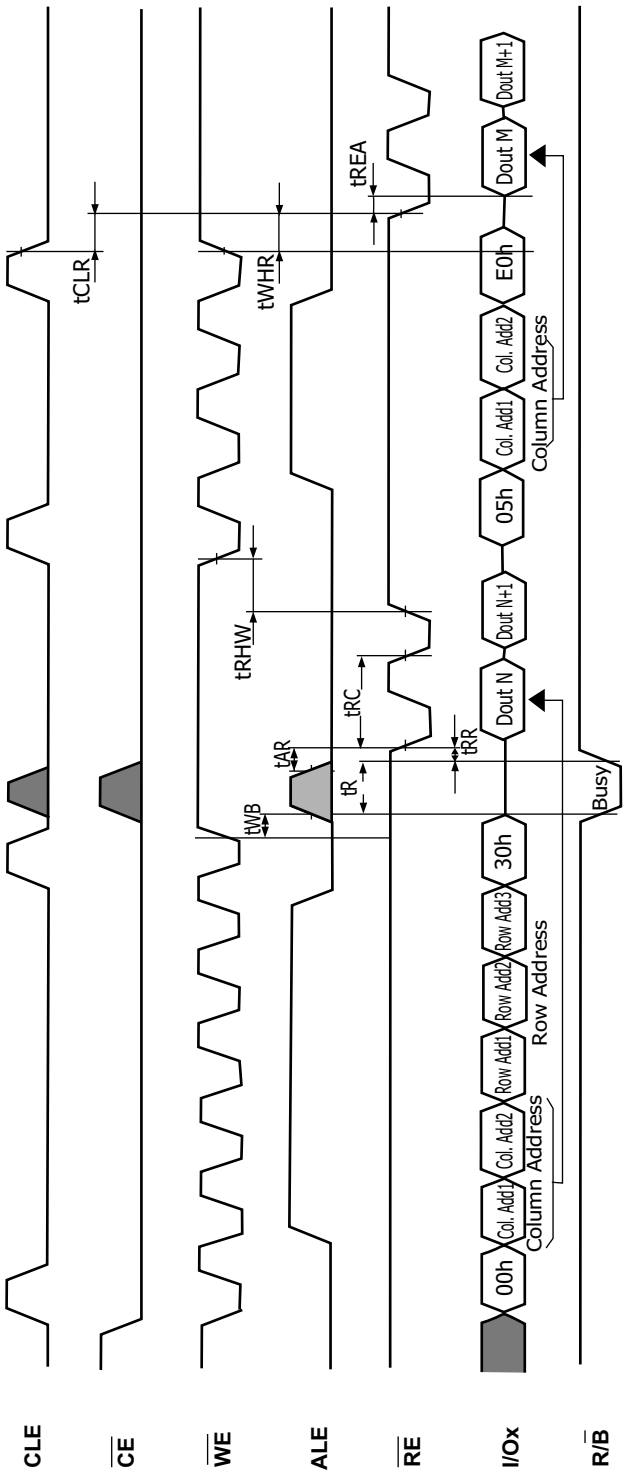


Figure 12 : Random Data output

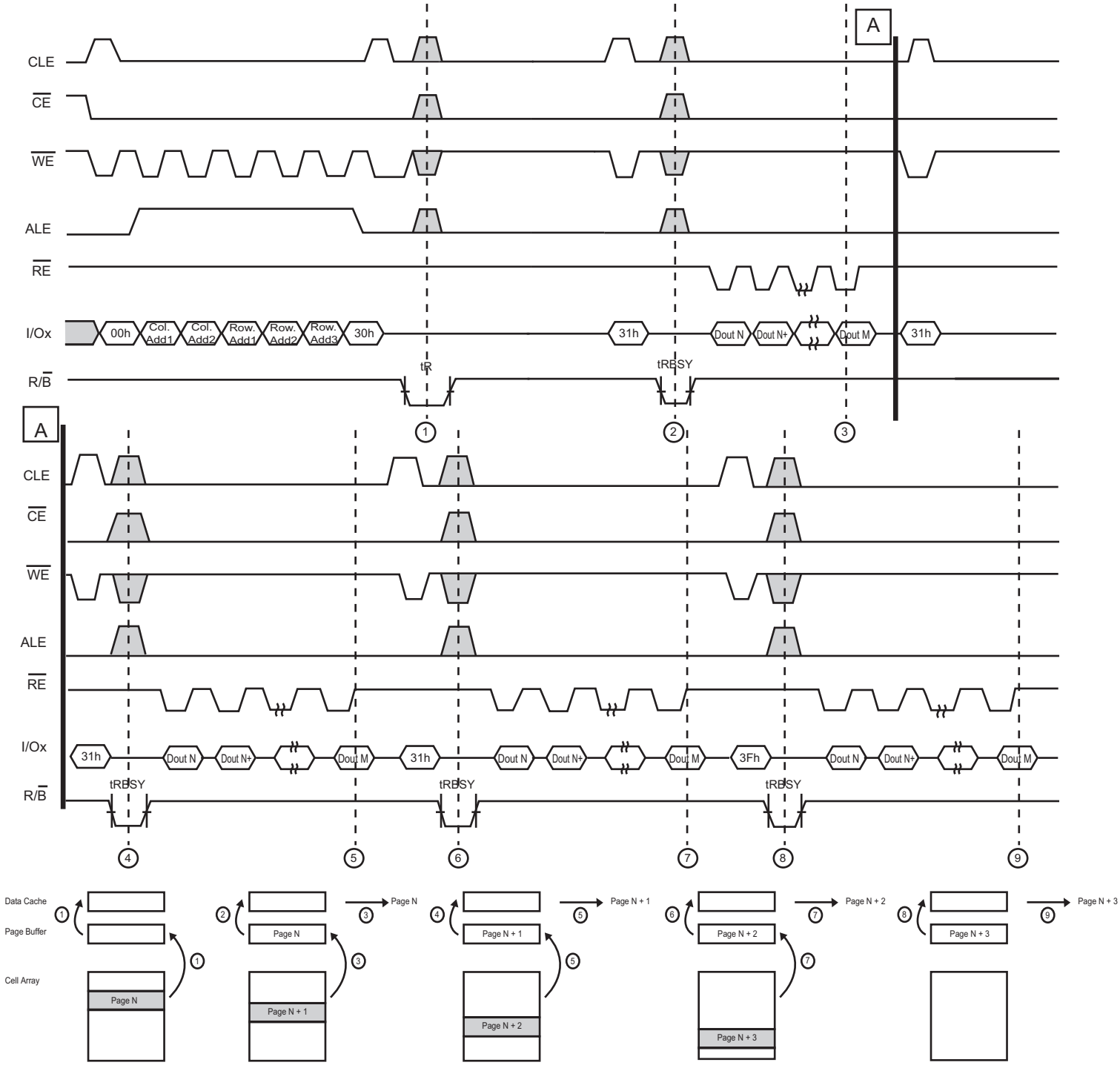
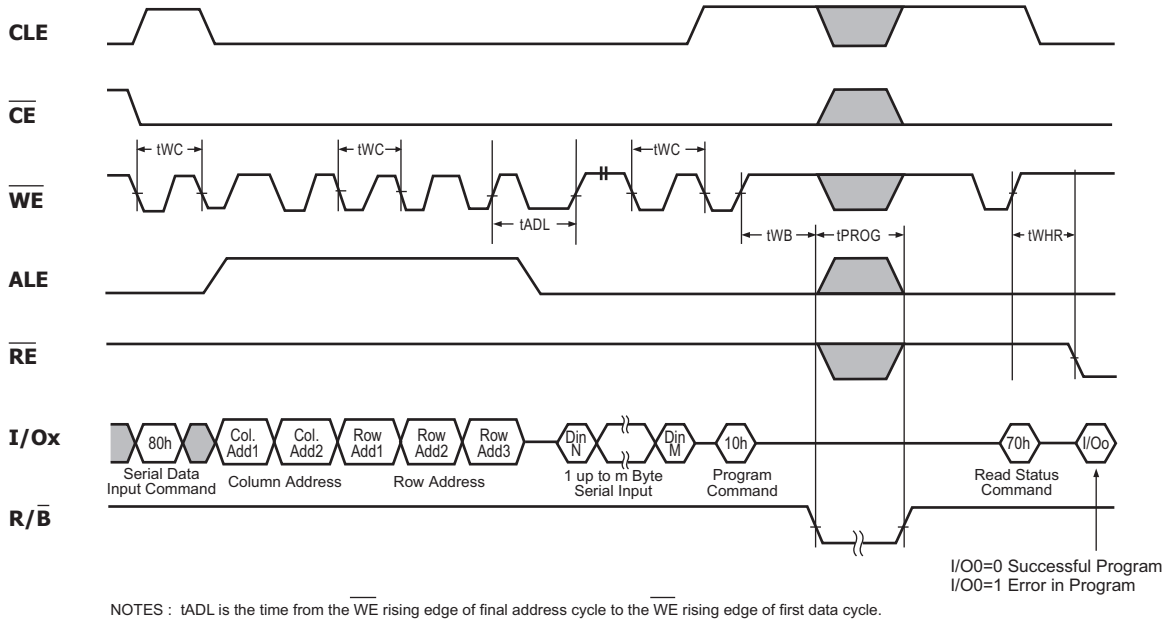


Figure 13: Read Operation with Read Cache



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 14: Page Program Operation

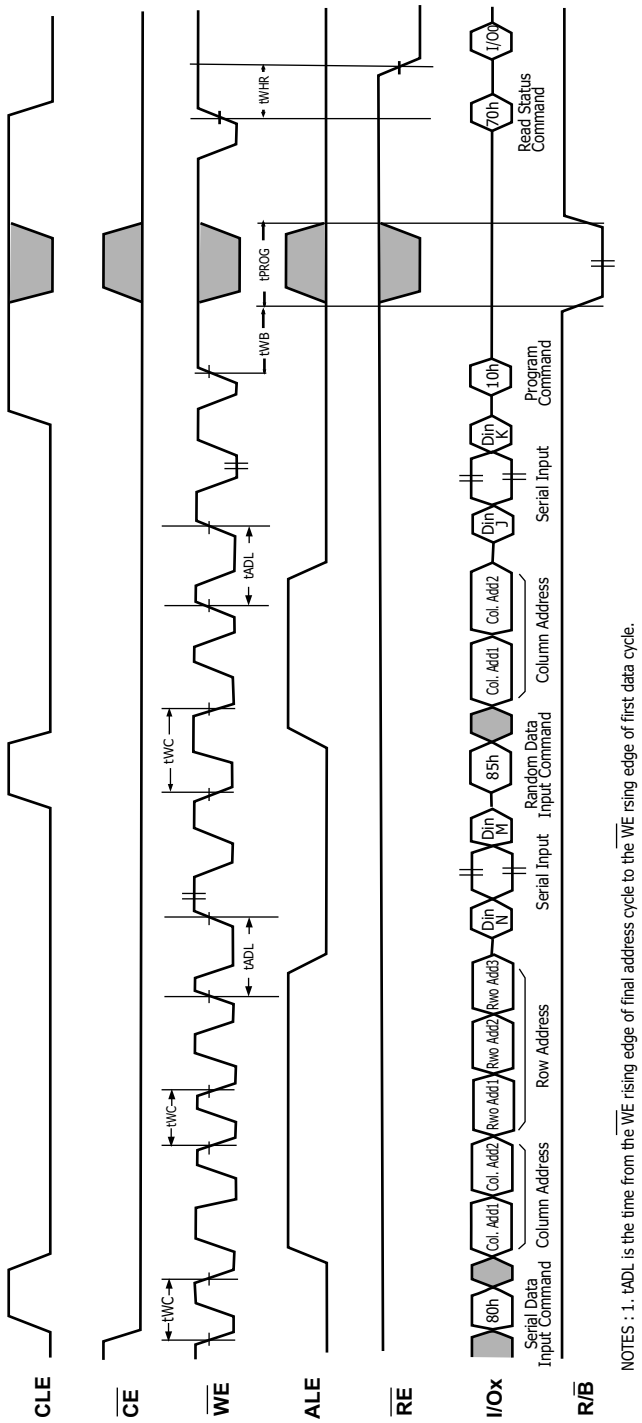


Figure 15 : Random Data In

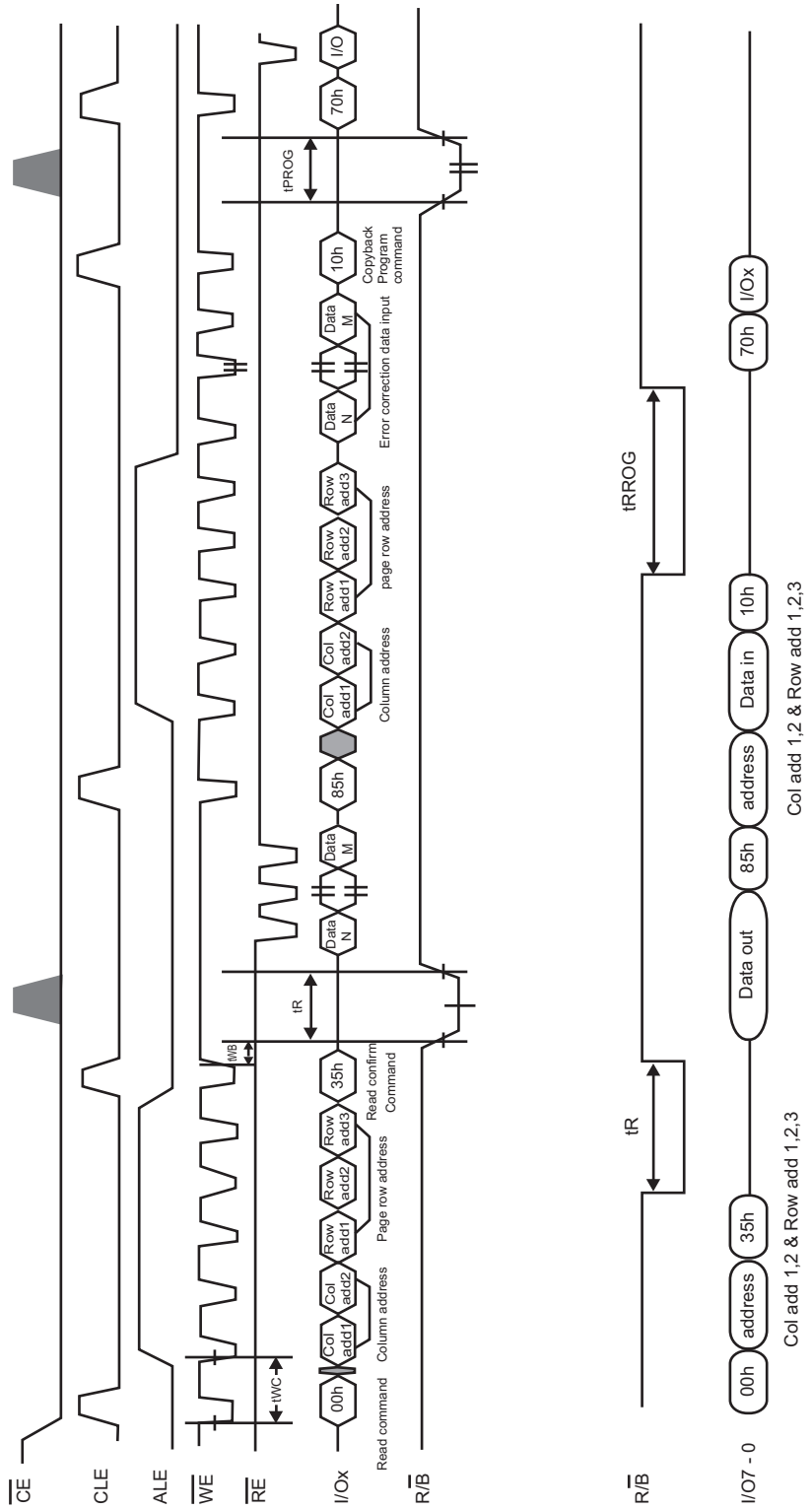


Figure 16: Copy Back Program Operation

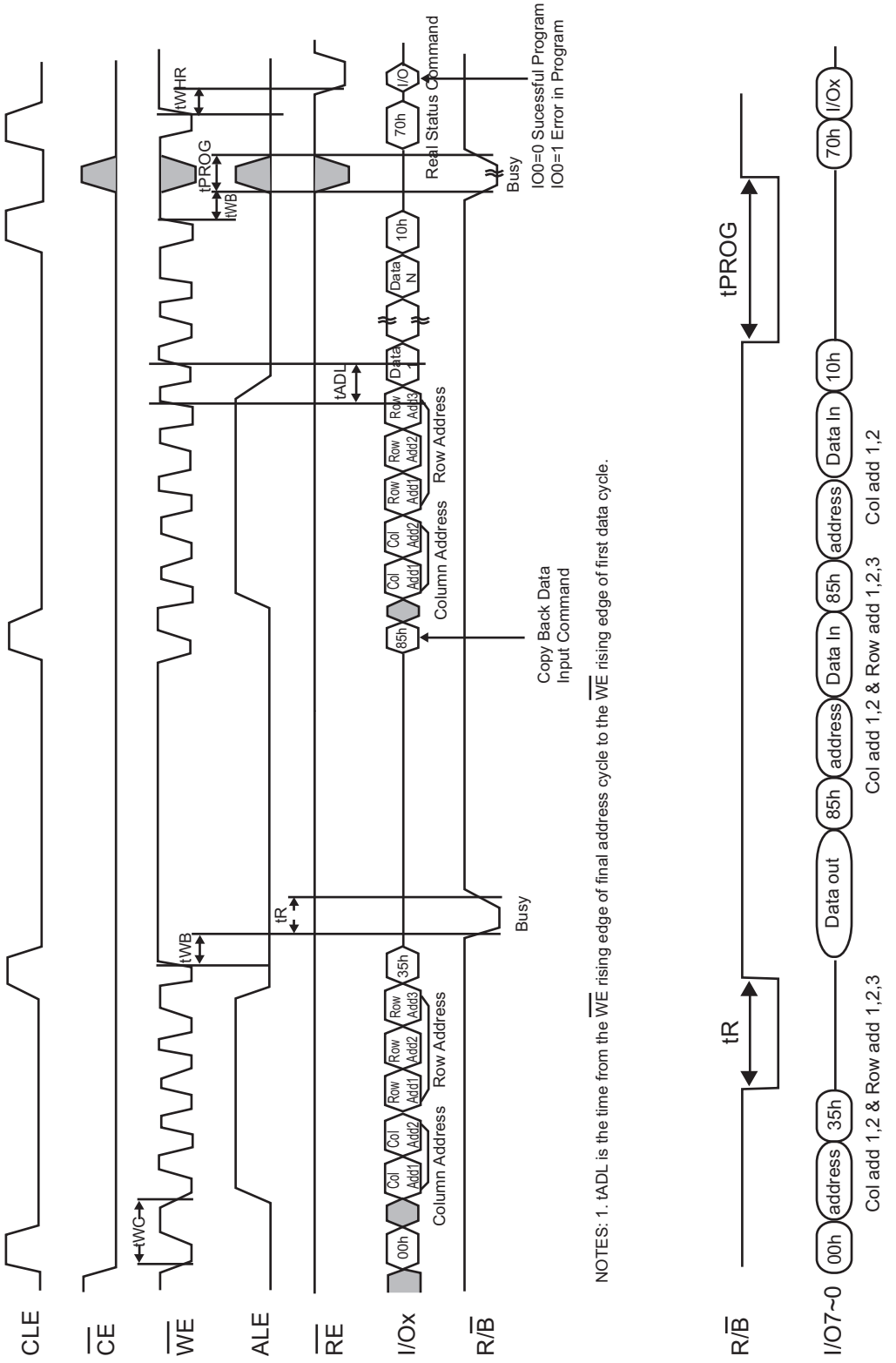


Figure 17: Copy Back Program Operation with Random Data Input

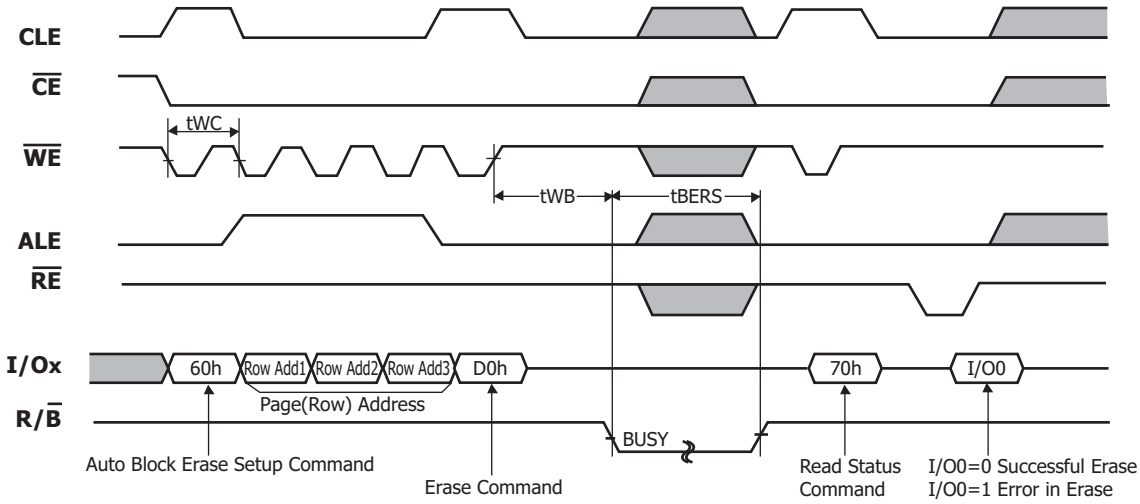


Figure 18: Block Erase Operation (Erase One Block)

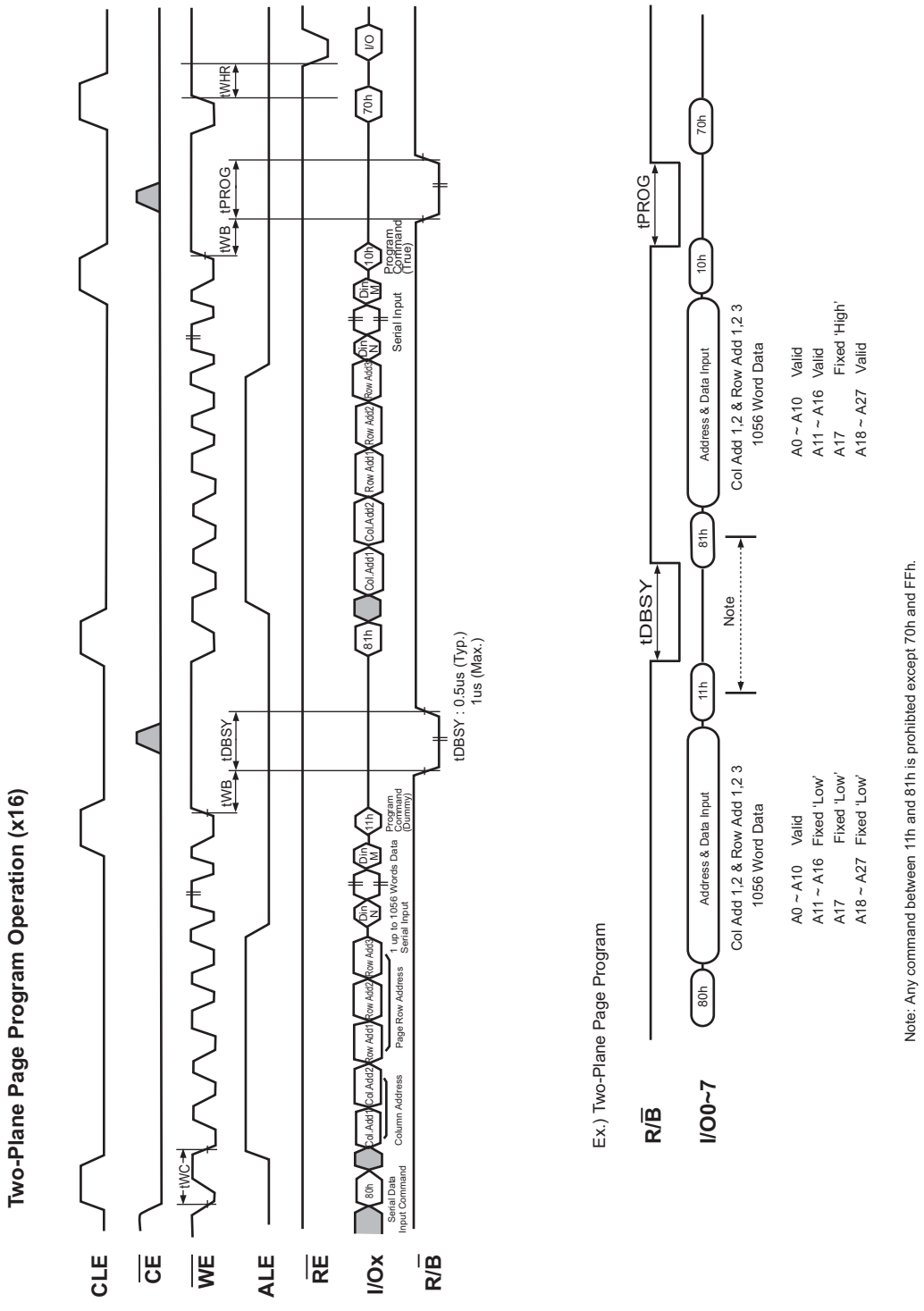
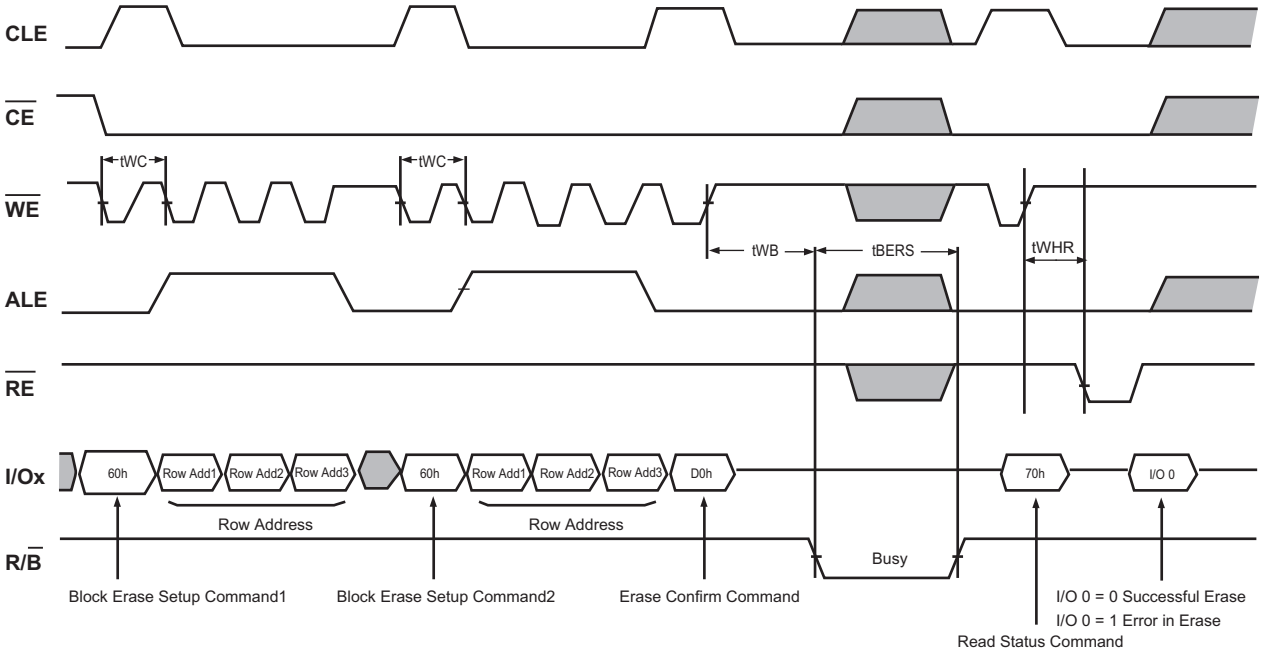


Figure 19: Multiple plane page program



Ex.) Address Restriction for Two-Plane Block Erase Operation

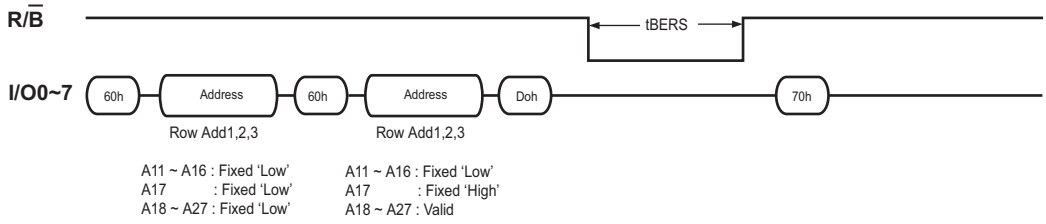
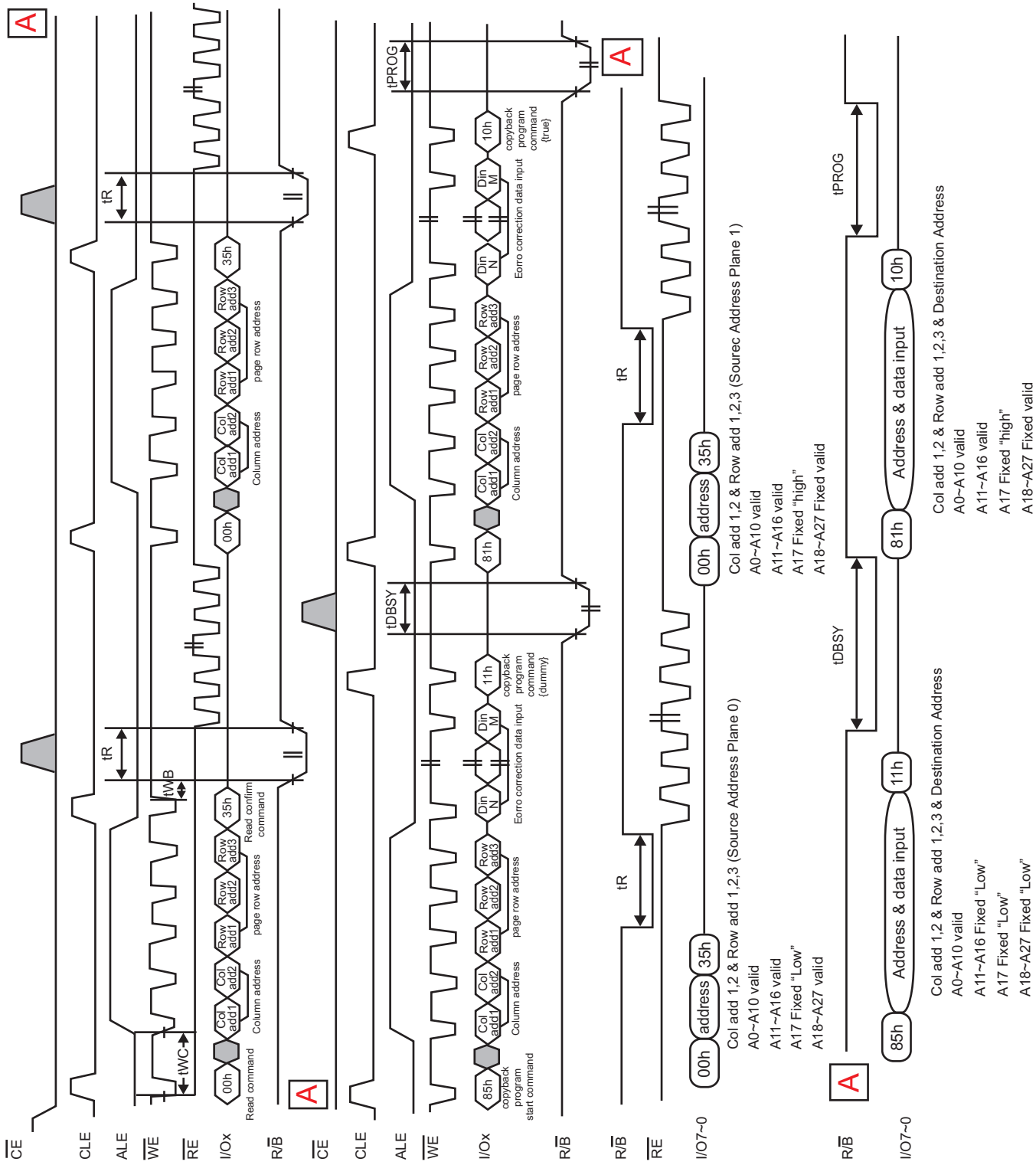


Figure 20 : Multiple plane erase operation



NOTE: Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 21: Multi plane copyback program Operation

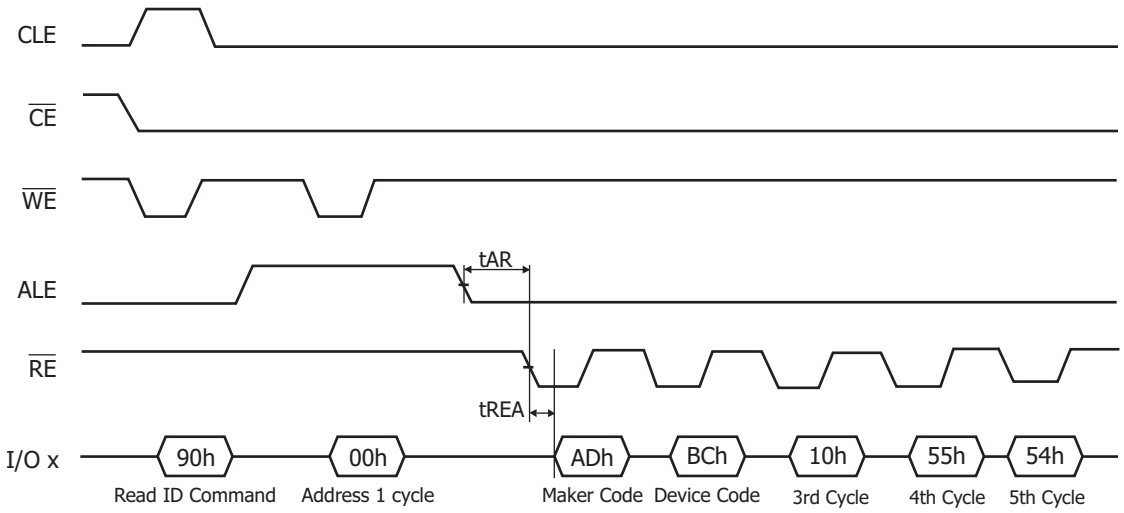


Figure 22: Read ID Operation

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ signal is ignored during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND

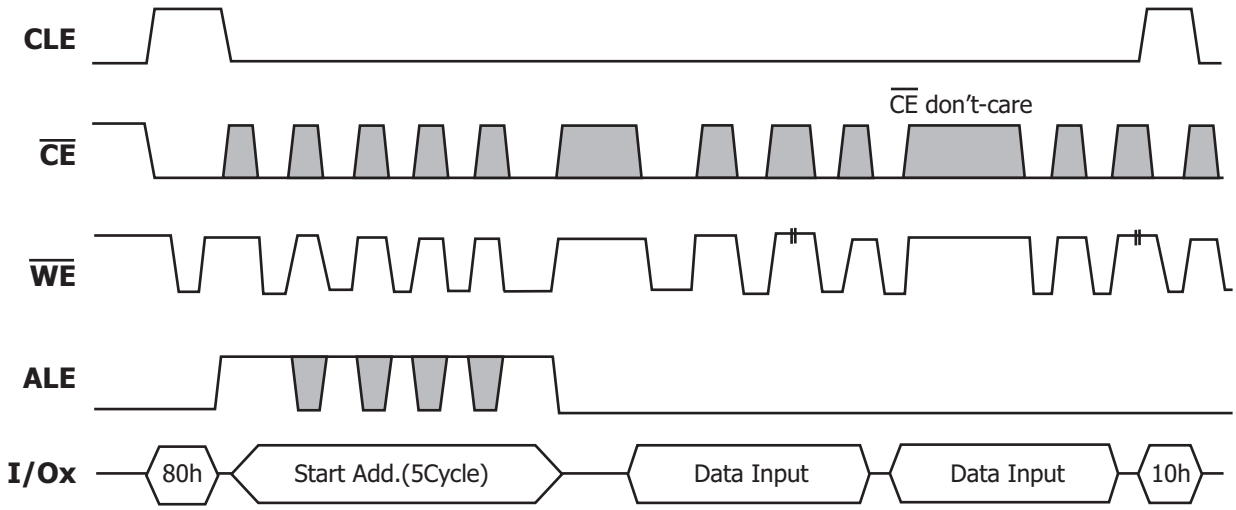


Figure 23: Program Operation with $\overline{CE}$ don't-care.

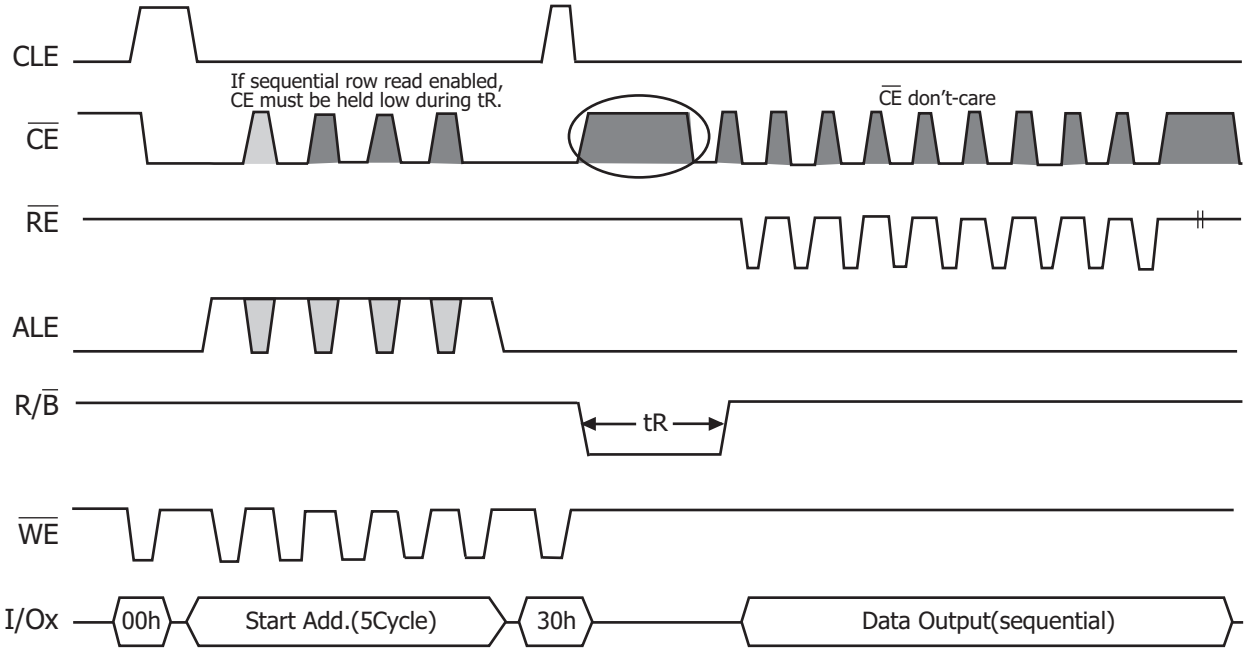


Figure 24: Read Operation with $\overline{CE}$ don't-care.

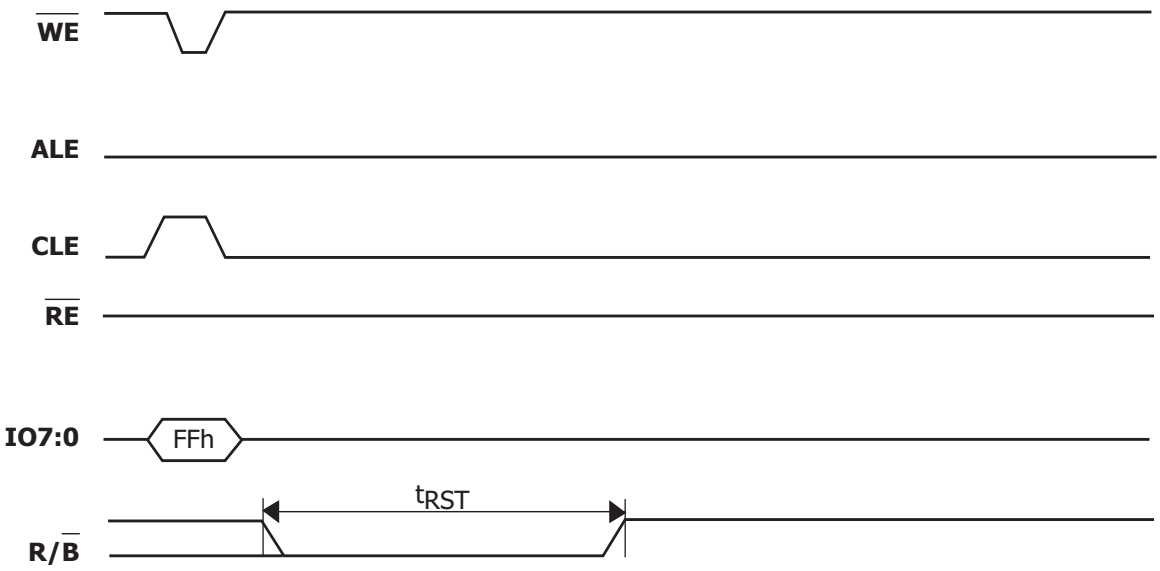


Figure 25: Reset Operation

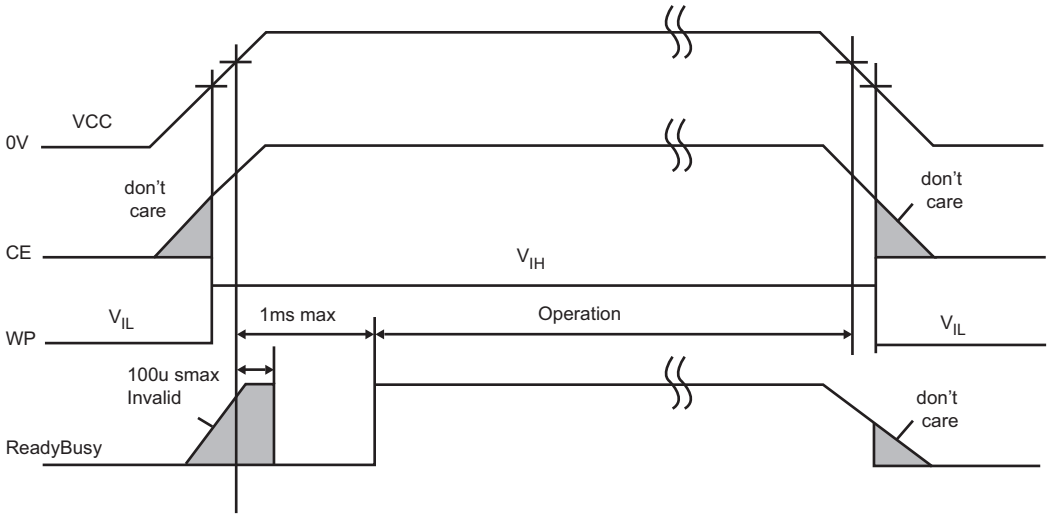


Figure 26: Power On and Data Protection Timing

VTH = 1.5 Volt for 1.8 Volt Supply devices

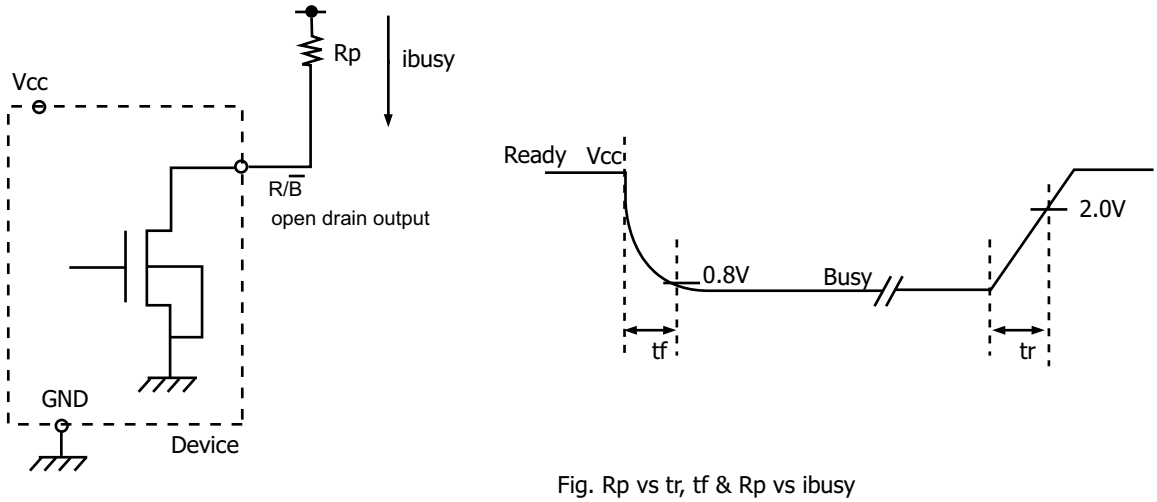
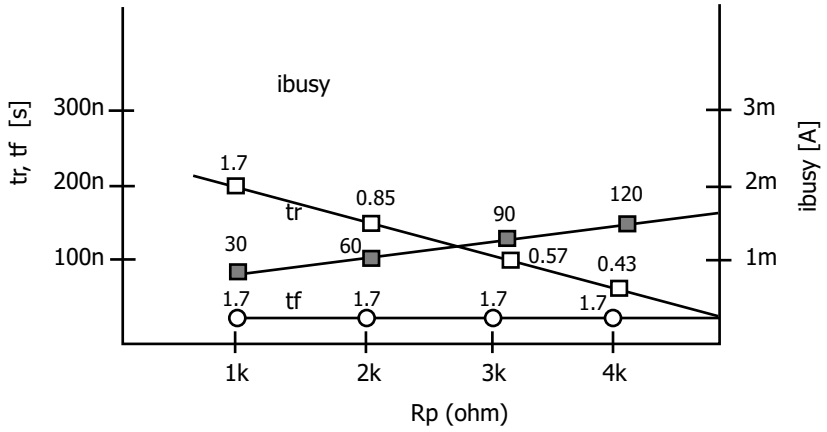


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 1.8V, Ta = 25°C, CL=30pF



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.85V}{3mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 27: Ready/Busy Pin electrical specifications

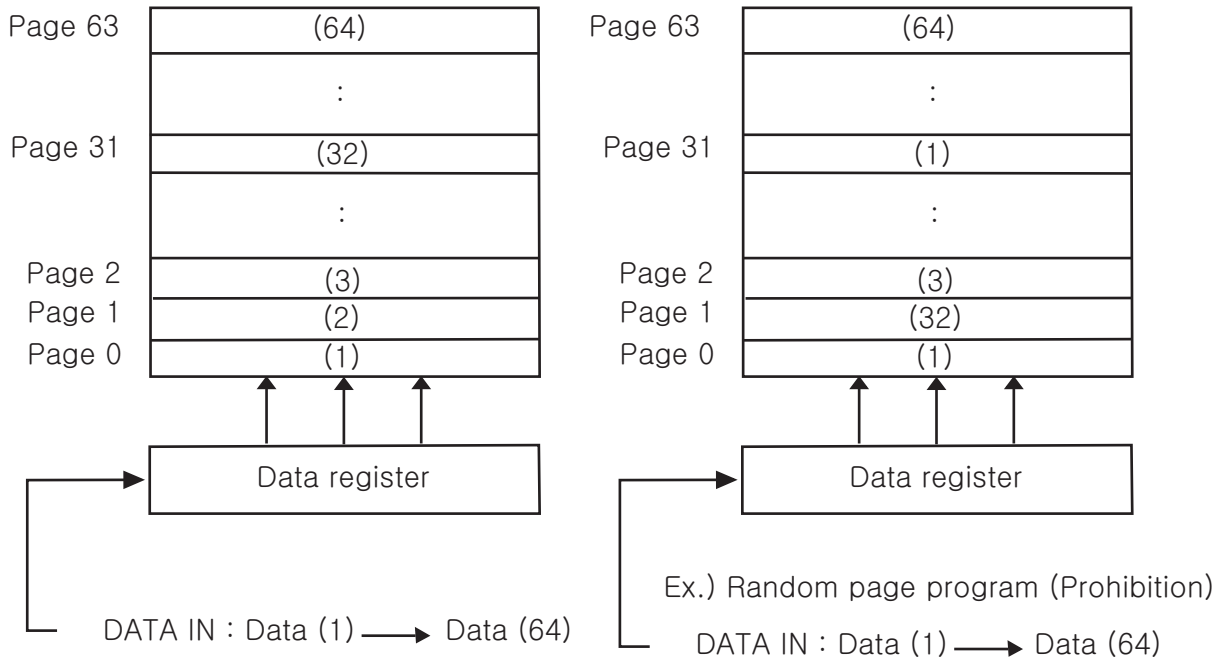


Figure 28: page programming within a block

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte(1st word) in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 29. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

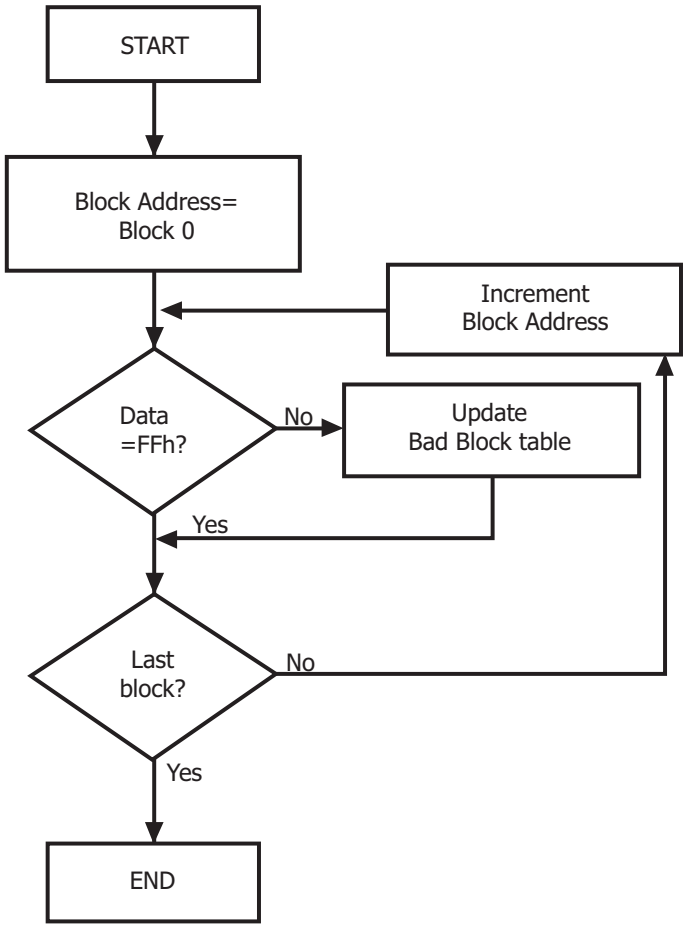


Figure 29: Bad Block Management Flowchart

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
Unlike the case of odd page which carries a possibility of affecting previous page, the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to Table 23 and Figure 30 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 1bit/528byte)

Table 23: Block Failure

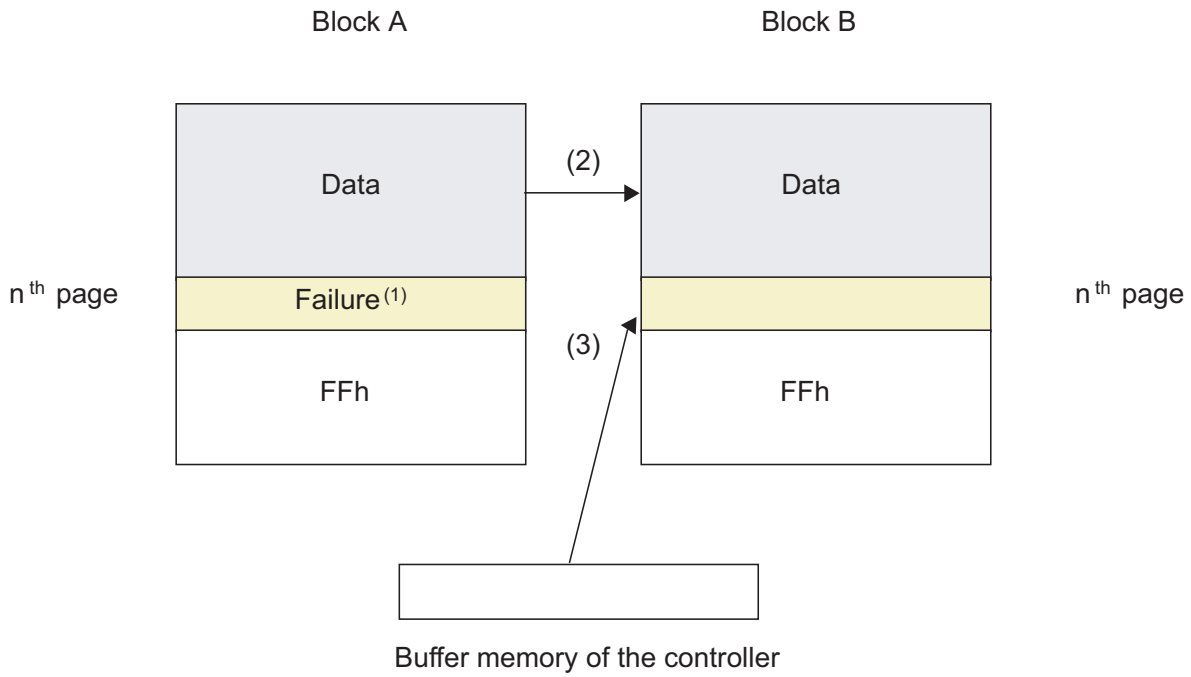


Figure 30: Bad Block Replacement

NOTE :
1. An error occurs on n^{th} page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from eraseing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 31~34)

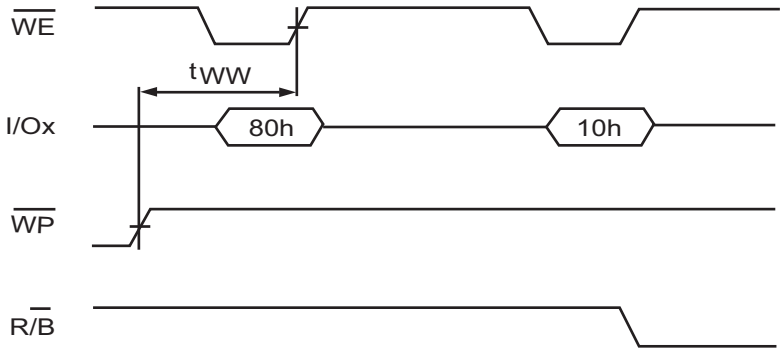


Figure 31: Enable Programming

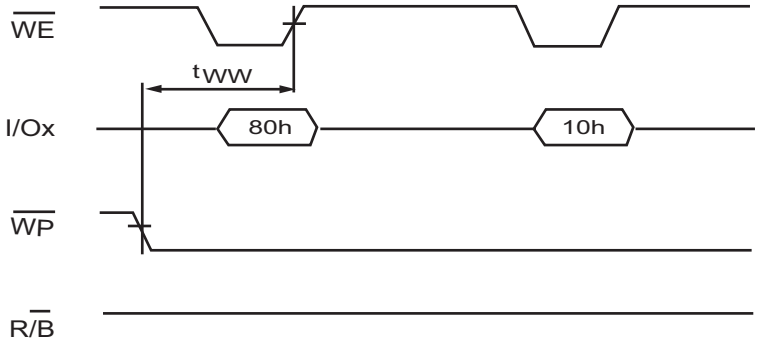


Figure 32: Disable Programming

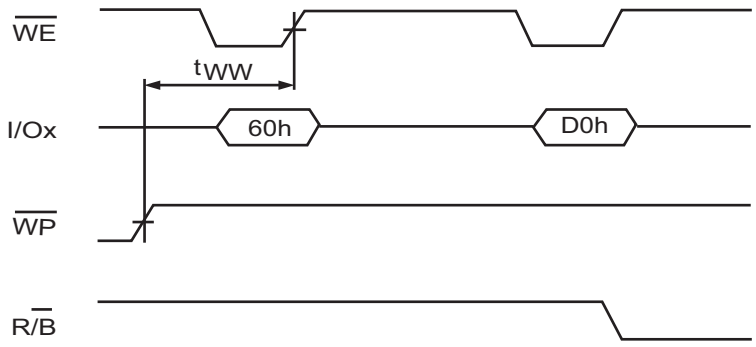


Figure 33: Enable Erasing

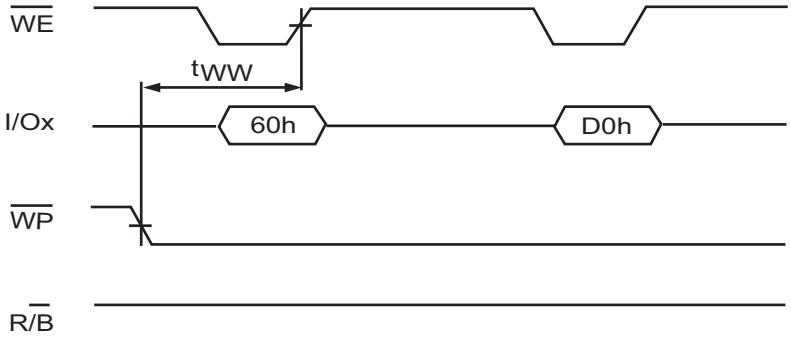


Figure 34: Disable Erasing

1Gb (64Mbx16) Mobile DDR A-Die

DESCRIPTION

The Hynix Mobile DRAM is 1,073,741,824-bit CMOS Low Power Double Data Rate Synchronous DRAM (Mobile DDR SDRAM), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 16,777,216 x16.

The Hynix Mobile DRAM is uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins.

The Hynix Mobile DRAM is offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (Mobile DDR SDRAM operates from a differential clock*: the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK*), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (*Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK*). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the Low Power DDR SDRAM (Mobile DDR SDRAM) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Low Power DDR SDRAM (Mobile DDR SDRAM) provides for programmable read or write bursts of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multibank architecture of Low Power DDR SDRAM (Mobile DDR SDRAM) allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

The Low Power DDR SDRAM (Mobile DDR SDRAM) also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half, quarter and 1/8 and 1/16 array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule). Only Read bursts in progress with auto precharge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Autoprecharge enabled and for Write bursts.

The Hynix Mobile DRAM is has the special Low Power function of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

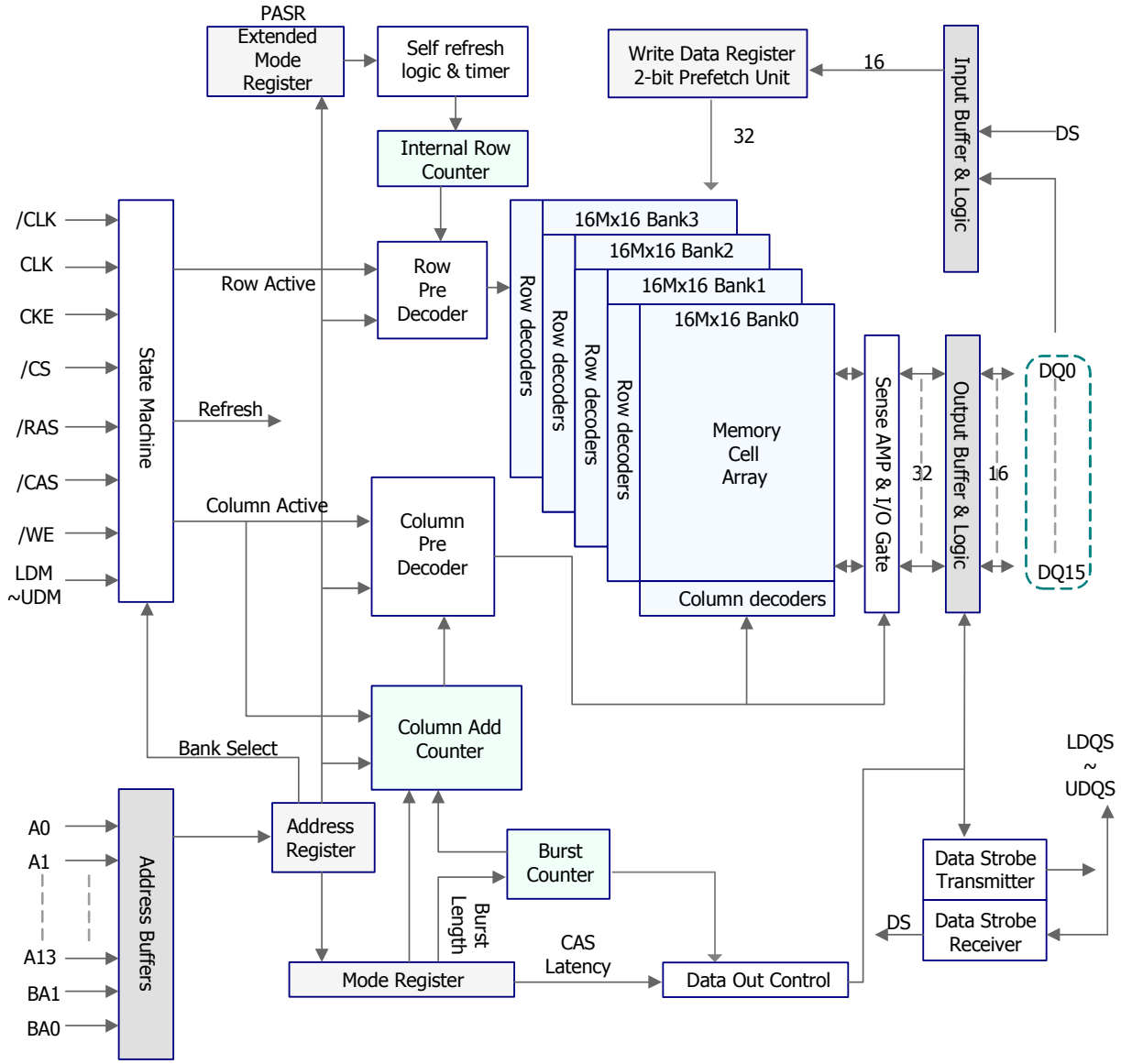
All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Mobile DDR SDRAM PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	INPUT	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	INPUT	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
$\overline{CS}$	INPUT	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered
BA0, BA1	INPUT	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS, EMRS).
A0 ~ A13	INPUT	Address inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. For 1Gb (x16), Row Address: A0 ~ A13, Column Address: A0 ~ A9 Auto-precharge flag: A10
DQ0 ~ DQ15	I/O	Data Bus: data input / output pin
LDM ~ UDM	INPUT	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, and UDM corresponds to the data on DQ8-DQ15.
LDQS ~ UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, and UDQS corresponds to the data on DQ8-DQ15.
V_{DD}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground
V_{DDQ}	SUPPLY	I/O Power supply
V_{SSQ}	SUPPLY	I/O Ground
NC	-	No Connect: No internal electrical connection is present.

FUNCTIONAL BLOCK DIAGRAM

4banks x 16Mbit x 16 I/O Mobile DDR SDRAM



REGISTER DEFINITION I

Mode Register Set (MRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Length		

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

REGISTER DEFINITION II

Extended Mode Register Set (EMRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS			0	0	PASR		

DS (Drive Strength)

A7	A6	A5	Drive Strength
0	0	0	Full(Default)
0	0	1	Half
0	1	0	Quarter
0	1	1	Octant
1	0	0	Three-Quarters

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks (Default)
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

COMMAND TRUTH TABLE

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Autoprecharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Autoprecharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all Banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op code		10

DM TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:
1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with auto precharge disabled. This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among MRS, EMRS and SRR.
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH.

CKE TRUTH TABLE

CKEn-1	CKEn	Current State	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,8
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,9
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	H	See the other Truth Tables			

Note:
1. CKEn is the logic state of CKE at clock edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LP DDR immediately prior to clock edge *n*.
3. COMMAND*n* is the command registered at clock edge n, and ACTION*n* is the result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The clock must toggle at least one time during the t_{XP} period.
9. The clock must toggle at least once during the t_{XSR} time.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *n*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start read burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto recharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met.
   Once tRCD is met, the bank will be in the "row active" state.
   Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met.
   Once tRFC is met, the LP DDR will be in an "all banks idle" state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
   Once tMRD is met, the LP DDR will be in an "all banks idle" state.
   Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *m*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Pre-charging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Case Temperature	TC	-30 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.3 ~ VDDQ+0.3	V
Voltage on VDD relative to VSS	VDD	-0.3 ~ 2.7	V
Voltage on VDDQ relative to VSS	VDDQ	-0.3 ~ 2.7	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	0.7	W

AC and DC OPERATING CONDITIONS

OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.7	1.8	1.95	V	1
I/O Supply Voltage	VDDQ	1.7	1.8	1.95	V	1
Operating Case Temperature	TC	-30		85	°C	

CLOCK INPUTS (CK, $\overline{CK}$)

Parameter	Symbol	Min	Max	Unit	Note
DC Input Voltage	VIN	-0.3	VDDQ+0.3	V	
DC Input Differential Voltage	VID(DC)	0.4*VDDQ	VDDQ+0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6*VDDQ	VDDQ+0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4*VDDQ	0.6*VDDQ	V	3

Address And Command Inputs (A0~An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH	0.8*VDDQ	VDDQ+0.3	V	
Input Low Voltage	VIL	-0.3	0.2*VDDQ	V	

Data Inputs (DQ, DM, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Input High Voltage	VIHD(DC)	0.7*VDDQ	VDDQ+0.3	V	
DC Input Low Voltage	VILD(DC)	-0.3	0.3*VDDQ	V	
AC Input High Voltage	VIHD(AC)	0.8*VDDQ	VDDQ+0.3	V	
AC Input Low Voltage	VILD(AC)	-0.3	0.2*VDDQ	V	

Data Outputs (DQ, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9*VDDQ	-	V	
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1*VDDQ	V	

Leakage Current

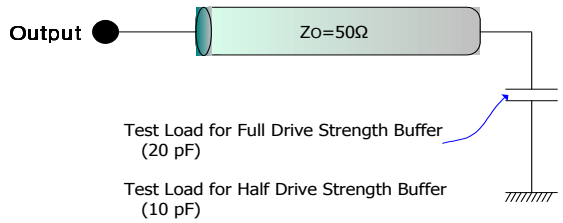
Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	4
Output Leakage Current	ILO	-1.5	1.5	uA	5

Note:
1. All voltages are referenced to VSS = 0V and VSSQ must be same potential and VDDQ must not exceed the level of VDD.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.
4. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.
5. DOUT is disabled. VOUT= 0 to 1.95V.

AC OPERATING TEST CONDITION

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.8*VDDQ/0.2*VDDQ	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note: 1. The circuit shown on the right represents the timing load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design and characterization. Use of IBIS or other simulation tools for system design validation is suggested.



Input / Output Capacitance

Parameter	Symbol	Speed		Unit	Note
		Min	Max		
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.5	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input/output capacitance, DQ, DM, DQS	CIO	2.0	4.5	pF	4

Note:
1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

Mobile DDR OUTPUT SLEW RATE CHARACTERRISTICS

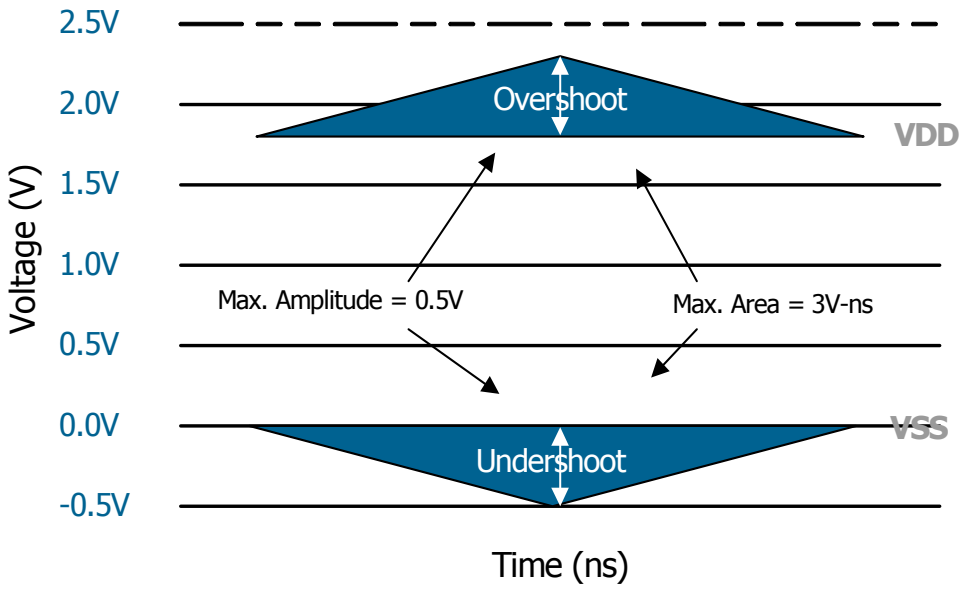
Parameter	Min	Max	Unit	Note
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1, 2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1, 2
Output Slew Rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

Note:
1. Measured with a test load of 20pF connected to VSSQ
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC)
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Mobile DDR AC OVERSHOOT / UNDERSHOOT SPECIFICATION

Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.5V
Maximum peak amplitude allowed for undershoot	0.5V
The area between overshoot signal and VDD must be less than or equal to	3V-ns
The area between undershoot signal and GND must be less than or equal to	3V-ns

Note:
1. This specification is intended for devices with no clamp protection and is guaranteed by design.



DC CHARACTERISTICS (Symbols)

Parameter	Symbol
Operating one bank active-precharge current	IDD0
Precharge power-down standby current	IDD2P
Precharge power-down standby current with clock stop	IDD2PS
Precharge non power-down standby current	IDD2N
Precharge non power-down standby current with clock stop	IDD2NS
Active power-down standby current	IDD3P
Active power-down standby current with clock stop	IDD3PS
Active non power-down standby current	IDD3N
Active non power-down standby current with clock stop	IDD3NS
Operating burst read current	IDD4R
Operating burst write current	IDD4W
Auto Refresh Current	IDD5
Self Refresh Current	IDD6

DC CHARACTERISTICS

Symbol	Test Condition	Max					Unit	Note
		DDR 400	DDR 370	DDR 333	DDR 266	DDR 200		
IDD0	tRC = tRC(min); tCK = tCK(min); CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	80	70	60	50	40	mA	1
IDD2P	all banks idle; CKE is LOW; $\overline{CS}$ is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	0.4					mA	
IDD2PS	all banks idle; CKE is LOW; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	0.4					mA	
IDD2N	all banks idle; CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	12					mA	
IDD2NS	all banks idle; CKE is HIGH; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	6						
IDD3P	one bank active; CKE is LOW; $\overline{CS}$ is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	3					mA	
IDD3PS	one bank active; CKE is LOW; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	2						
IDD3N	one bank active; CKE is HIGH; $\overline{CS}$ is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	12					mA	
IDD3NS	one bank active; CKE is HIGH; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	8					mA	
IDD4R	one bank active; BL=4; CL=3; tCK=tCK(min); continuous read bursts; I_{OUT}=0mA; address inputs are SWITCHING, 50% data change each burst transfer	135	100	90	80	70	mA	1
IDD4W	one bank active; BL=4; tCK=tCK(min); continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	130	95	85	75	65	mA	
IDD5	tRC=tRFC(min); tCK=tCK(min); burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	200					mA	tRFC= 72ns
		120						tRFC= 110ns
		110						tRFC= 138ns
IDD6	CKE is LOW; CK=LOW; $\overline{CK}$=HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	See Next Page					uA	2

Note:
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is 1V/ns
3. Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$
   STABLE is defined as inputs stable at a HIGH or LOW level
   SWITCHING is defined as
   - address and command: inputs changing between HIGH and LOW once per two clock cycles
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle
     DM and DQS are STABLE
4. All IDD values are guaranteed by full range of operating voltage and temperature.
   VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30°C ~ +85°C

DC CHARACTERISTICS - IDD6

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
45	450	350	300	uA
85	900	650	500	uA

Note:
1. Related numerical values in this 45°C are examples for reference sample value only.
2. With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.

AC CHARACTERISTICS (Symbols - Sheet 1 of 2)

Parameter		Symbol	Unit
DQ Output Access Time (from CK, $\overline{CK}$)		tAC	ns
DQS Output Access Time (from CK, $\overline{CK}$)		tDQSCK	ns
Clock High-level Width		tCH	tCK
Clock Low-level Width		tCL	tCK
Clock Half Period		tHP	ns
System Clock Cycle Time	CL = 3	tCK3	ns
	CL = 2	tCK2	ns
DQ and DM Input Setup Time		tDS	ns
DQ and DM Input Hold Time		tDH	ns
DQ and DM Input Pulse Width		tDIPW	ns
Address and Control Input Setup Time		tIS	ns
Address and Control Input Hold Time		tIH	ns
Address and Control Input Pulse Width		tIPW	ns
DQ & DQS Low-impedance time from CK, $\overline{CK}$		tLZ	ns
DQ & DQS High-impedance time from CK, $\overline{CK}$		tHZ	ns
DQS - DQ Skew		tDQSQ	ns
DQ / DQS output hold time from DQS		tQH	ns
Data Hold Skew Factor		tQHS	ns
Write Command to 1st DQS Latching Transition		tDQSS	tCK
DQS Input High-Level Width		tDQSH	tCK
DQS Input Low-Level Width		tDQSL	tCK
DQS Falling Edge of CK Setup Time		tDSS	tCK
DQS Falling Edge Hold Time from CK		tDSH	tCK

AC CHARACTERISTICS (Symbols - Sheet 2 of 2)

Parameter		Symbol	Unit
MODE REGISTER SET Command Period		tMRD	tCK
Write Preamble Setup Time		tWPRES	ns
Write Postamble		tWPST	tCK
Write Preamble		tWPRE	tCK
Read Preamble	CL = 3	tRPRE3	tCK
	CL = 2	tRPRE2	tCK
Read Postamble		tRPST	tCK
ACTIVE to PRECHARGE Command Period		tRAS	ns
ACTIVE to ACTIVE Command Period		tRC	ns
AUTO REFRESH to ACTIVE/AUTO REFRESH Command Period		tRFC	ns
ACTIVE to READ or WRITE Delay		tRCD	ns
PRECHARGE Command Period		tRP	ns
ACTIVE Bank *A* to ACTIVE Bank *B* Delay		tRRD	ns
WRITE Recovery Time		tWR	ns
Auto Precharge Write Recovery + Precharge Time		tDAL	tCK
Internal Write to Read Command Delay		tWTR	tCK
Self Refresh Exit to next valid Command Delay		tXSR	ns
Exit Power Down to next valid Command Delay		tXP	ns
CKE *min.* Pulse Width (High and Low)		tCKE	tCK
Average Periodic Refresh Interval		tREFI	us
Refresh Period		tREF	ms

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 1 of 2)

Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tAC	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tDQSCK	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tHP	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	ns	1,2
tCK3	5	-	5.4	-	6.0	-	7.5	-	10	-	ns	3
tCK2	12	-	12	-	12	-	12	-	15	-	ns	
tDS	0.48	-	0.54	-	0.6	-	0.8	-	1.1	-	ns	4,5,6
tDH	0.48	-	0.54	-	0.6	-	0.8	-	1.1	-	ns	4,5,6
tDIPW	1.8	-	1.8	-	1.8	-	1.8	-	2.2	-	ns	7
tIS	0.9	-	1.0	-	1.1	-	1.3	-	1.5	-	ns	6,8,9
tIH	0.9	-	1.0	-	1.1	-	1.3	-	1.5	-	ns	6,8,9
tIPW	2.3	-	2.3	-	2.3	-	2.6	-	3.0	-	ns	7
tLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	10
tHZ	-	5.0	-	5.0	-	5.0	-	6.0	-	7.0	ns	10
tDQSQ	-	0.4	-	0.45	-	0.5	-	0.6	-	0.7	ns	11
tQH	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	ns	2
tQHS	-	0.5	-	0.5	-	0.65	-	0.75	-	1.0	ns	2
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
tDQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	
tDQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	
tDSS	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK	
tDSH	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 2 of 2)

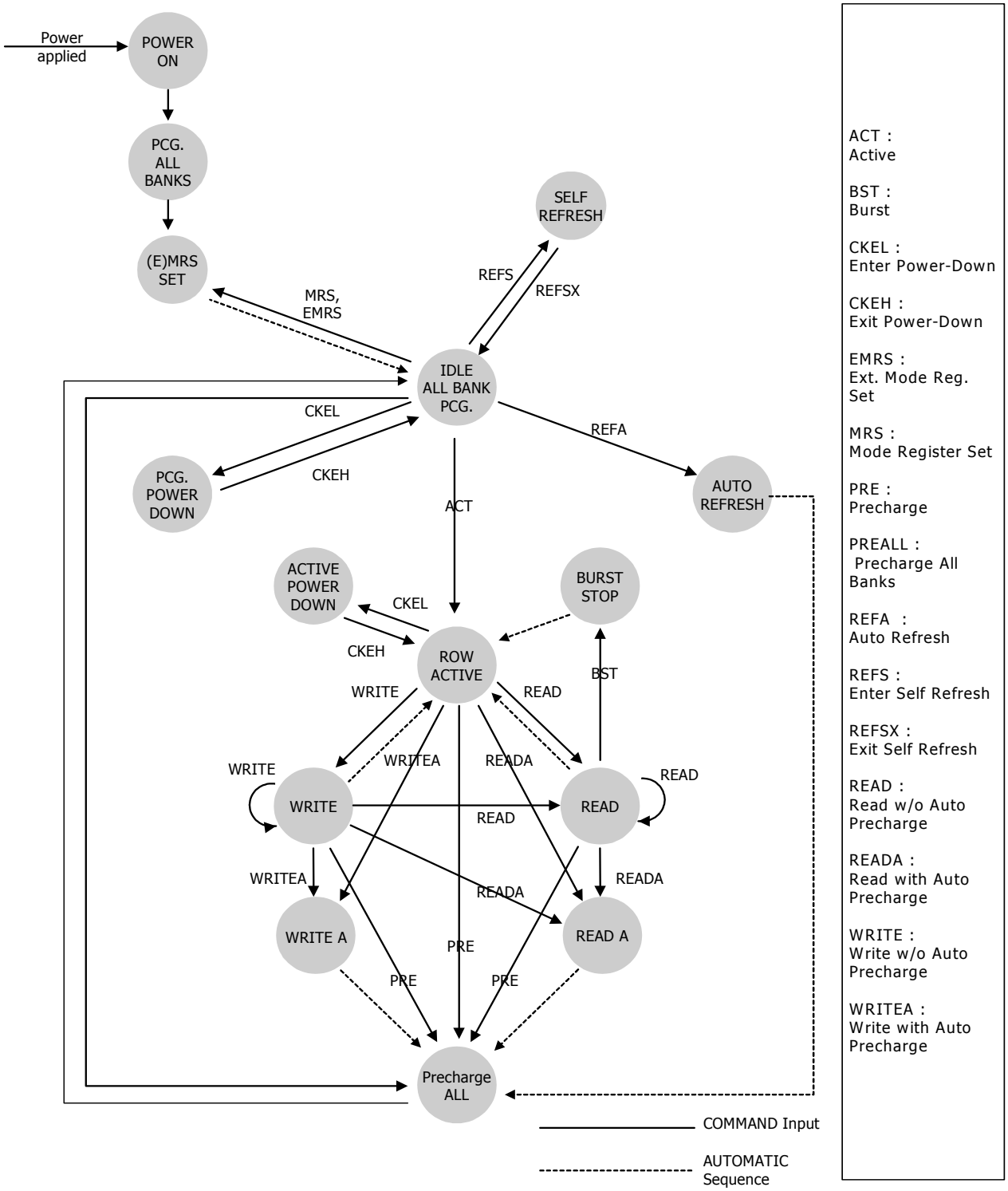
Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
tWPRES	0	-	0	-	0	-	0	-	0	-	ns	12
tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	13
tWPRE	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
tRPRE3	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	14
tRPRE2	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	tCK	14
tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRAS	40	70,000	42	70,000	42	70,000	45	70,000	50	70,000	ns	
tRC	55	-	58.2	-	60	-	75	-	80	-	ns	
tRFC	72	-	72	-	72	-	72	-	72	-	ns	
tRCD	20	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRP	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRRD	10	-	10.8	-	12	-	15	-	15	-	ns	
tWR	12	-	12	-	12	-	12	-	12	-	ns	
tDAL	(tWR/tCK) + (tRP/tCK)										tCK	16
tWTR	2	-	2	-	1	-	1	-	1	-	tCK	
tXSR	140	-	140	-	140	-	140	-	140	-	ns	
tXP	1CLK	-	1CLK	-	1CLK	-	1CLK	-	1CLK	-	ns	
tCKE	1	-	1	-	1	-	1	-	1	-	tCK	
tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	17
tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note:

1. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH})
2. t_{QH} = t_{HP} - t_{QHS}, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for
   1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
4. The transition time for DQ, DM and DQS inputs is measured between V_{IL}(DC) to V_{IH}(AC) for rising input signals, and V_{IH}(DC) to V_{IL}(AC) for falling input signals.
5. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
6. Input slew rate ≥ 1.0 V/ns.
7. These parameters guarantee device timing but they are not necessarily tested on each device.
8. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
9. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
10. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
11. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
15. Speed bin (CL-tRCD-tRP) = 3-3-3 for DDR200, DDR266, DDR333 and DDR370. Speed bin (CL-tRCD-tRP) = 3-4-3 for DDR400
16. Minimum 3CLK of tDAL(= tWR+tRP) is required because it need minimum 2CLK for tWR and minimum 1CLK for tRP.
    t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.
17. A maximum of eight Refresh commands can be posted to any given Low Power DDR SDRAM (Mobile DDR SDRAM), meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*t_{REFI}.
18. All AC parameters are guaranteed by full range of operating voltage and temperature.
    VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30^{o}C ~ +85^{o}C.
19. There must be at least one clock pulse during the tXP period. Please refer to the 'Power Down Mode' Section

Mobile DDR SDRAM OPERATION

State Diagram



DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

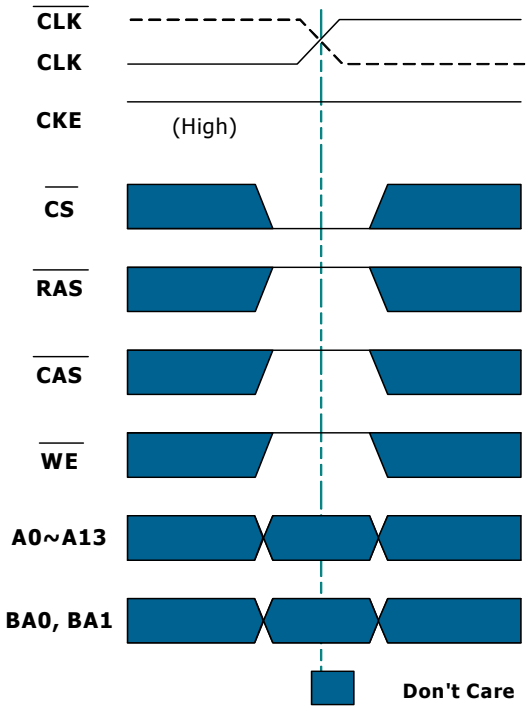
NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a Mobile DDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

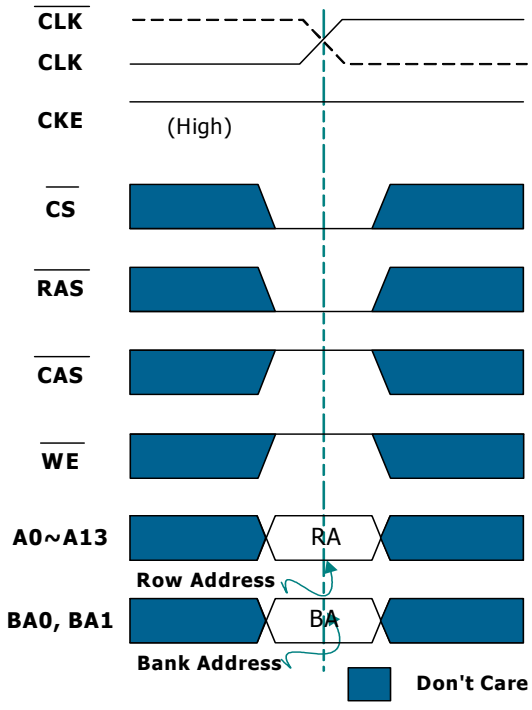
ACTIVE

The Active command is used to activate a row in a particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A13 (or the highest address bit) selects the row. (see to next figure)

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.
The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.
A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.



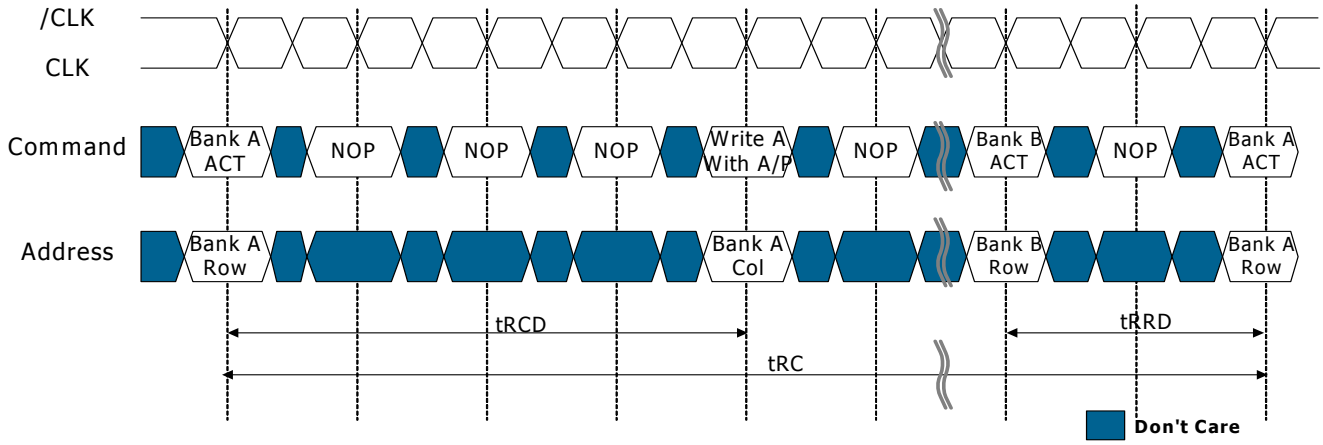
NOP Command



ACTIVE Command

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (*MIN*) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

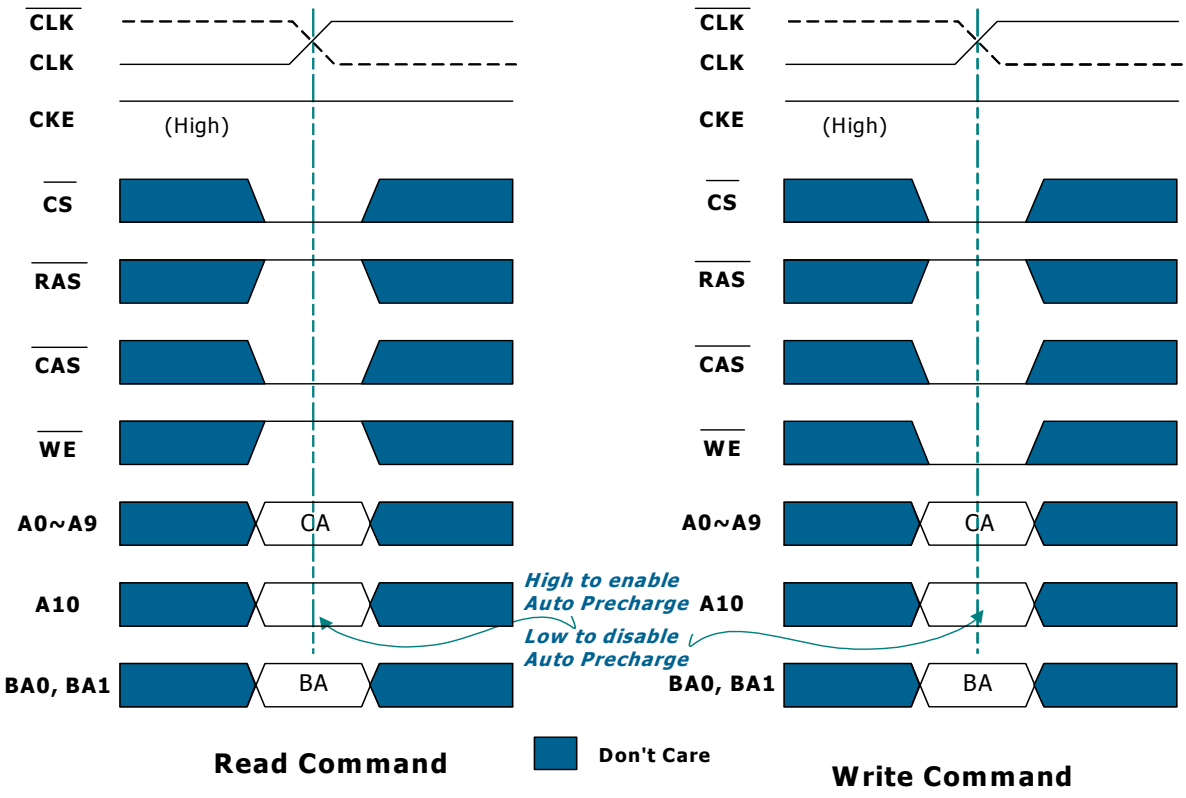


Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

READ / WRITE COMMAND

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued. The Mobile DDR drives the DQS during read operations. The initial low state of the DQS is known as the read preamble and the last data-out element is coincident with the read postamble. DQS is edge-aligned with read data. Upon completion of a burst, assuming no new READ commands have been initiated, the I/O's will go high-Z.

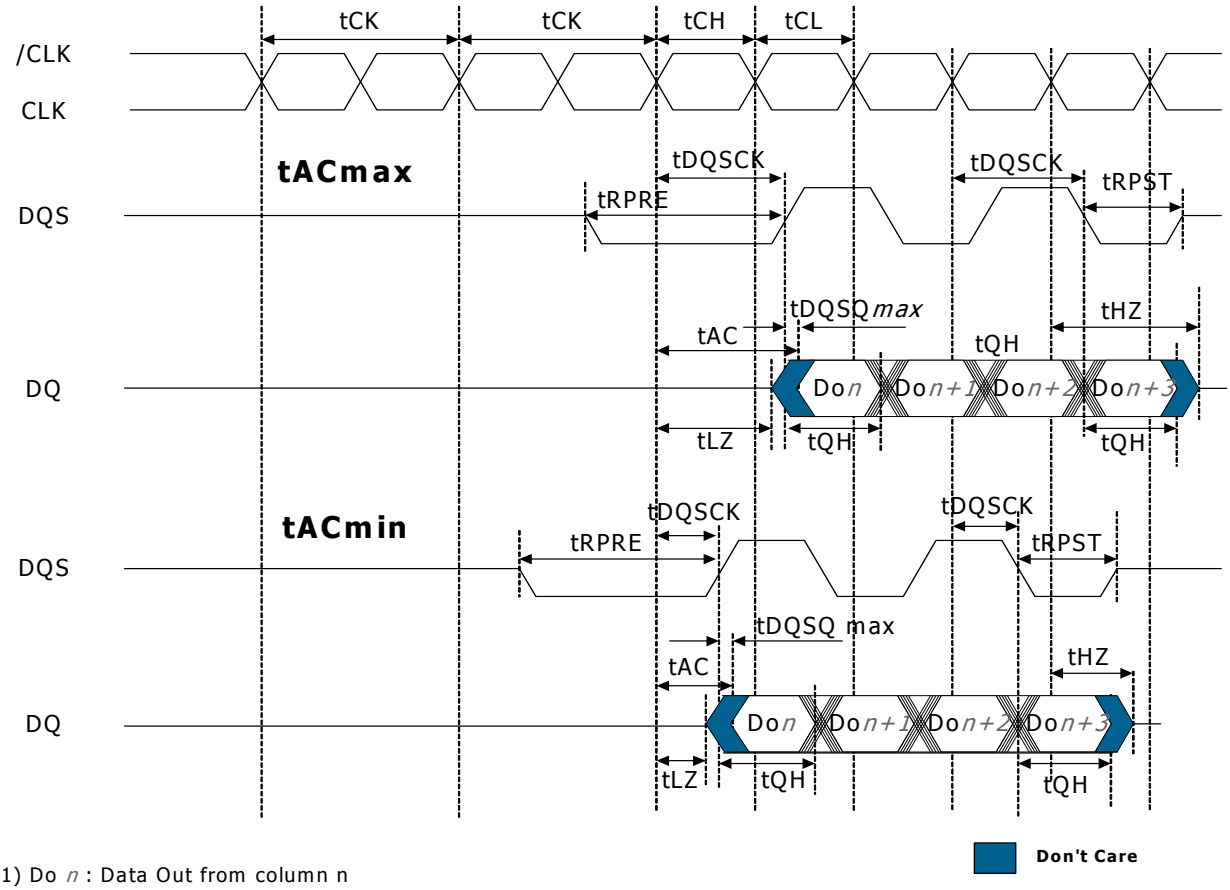
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used.If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access. Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to the memory; if the DM signal is registered high, the corresponding data-inputs will be ignored, and a write will not be executed to that byte/column location. The memory controller drives the DQS during write operations. The initial low state of the DQS is known as the write preamble and the low state following the last data-in element is write postamble. Upon completion of a burst, assuming no new commands have been initiated, the I/O's will stay high-Z and any additional input data will be ignored.



READ / WRITE COMMAND

READ

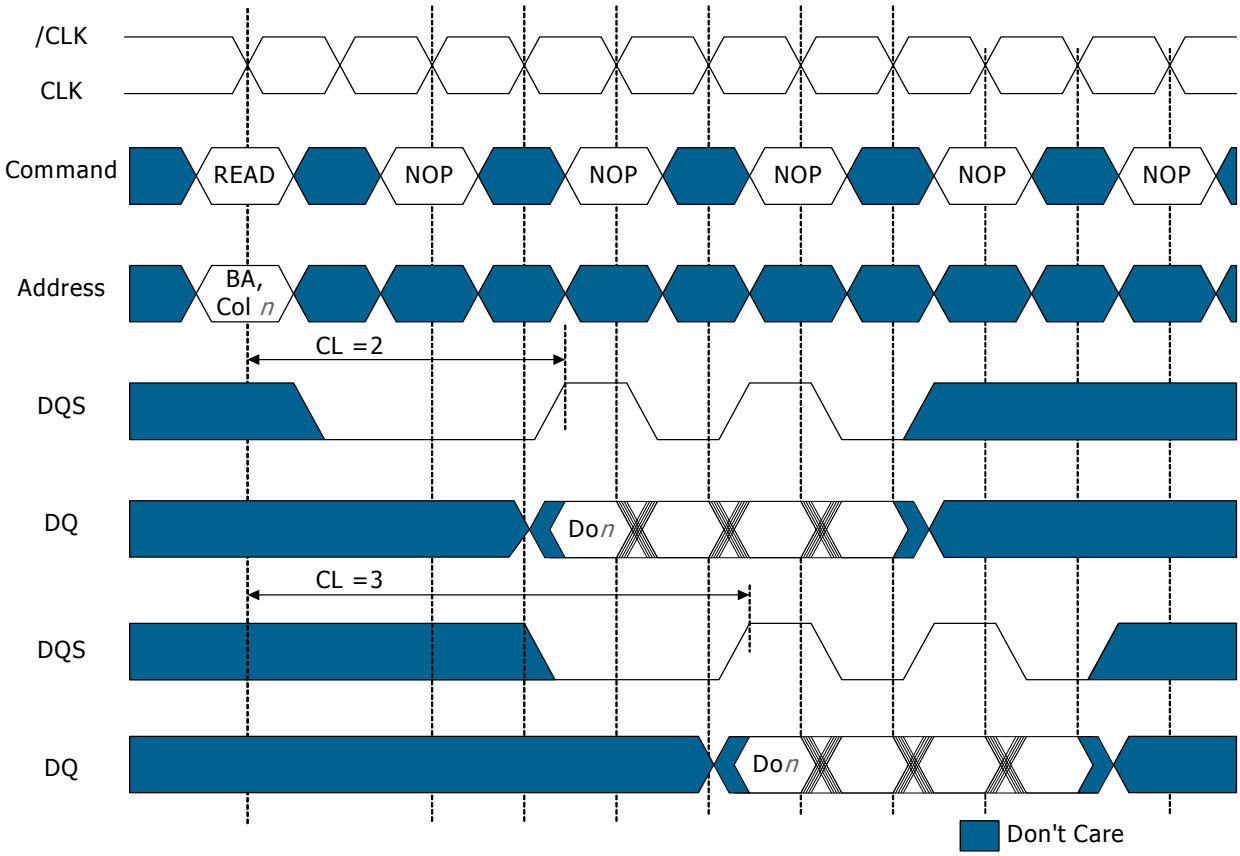
The basic Read timing parameters for DQ are shown next figure (Basic Read Timing Parameters). They apply to all Read operations. During Read bursts, DQS is driven by the Mobile DDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble.



1) Do *n* : Data Out from column n
2) All DQ are vaild tAC after the CK edge
   All DQ are vaild tDQSQ after the DQS edge, regardless of tAC

Basic Read Timing Parameters

The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in next figure with a CAS latency of 2 and 3.
Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

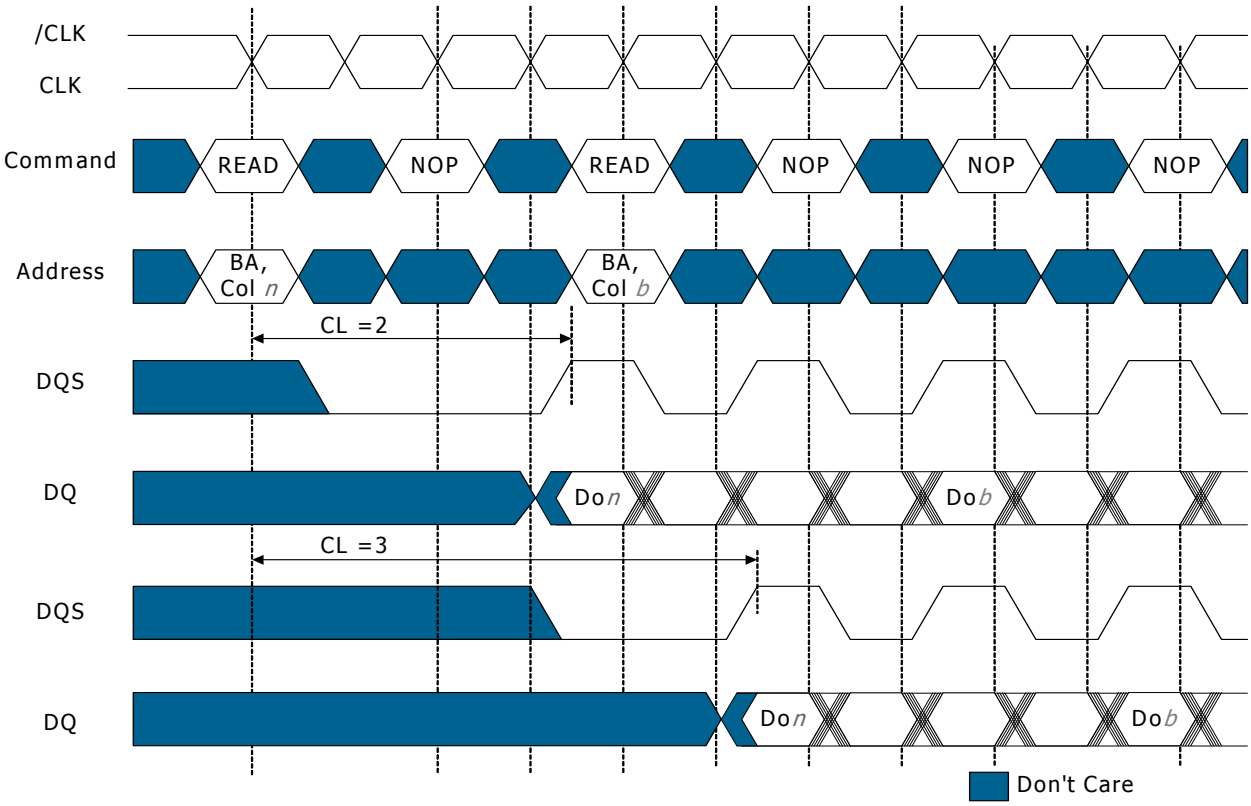


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 4; 3 subseqnent elements of Data Out appear in the programmed order following Do *n*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Read Burst Showing CAS Latency

READ to READ

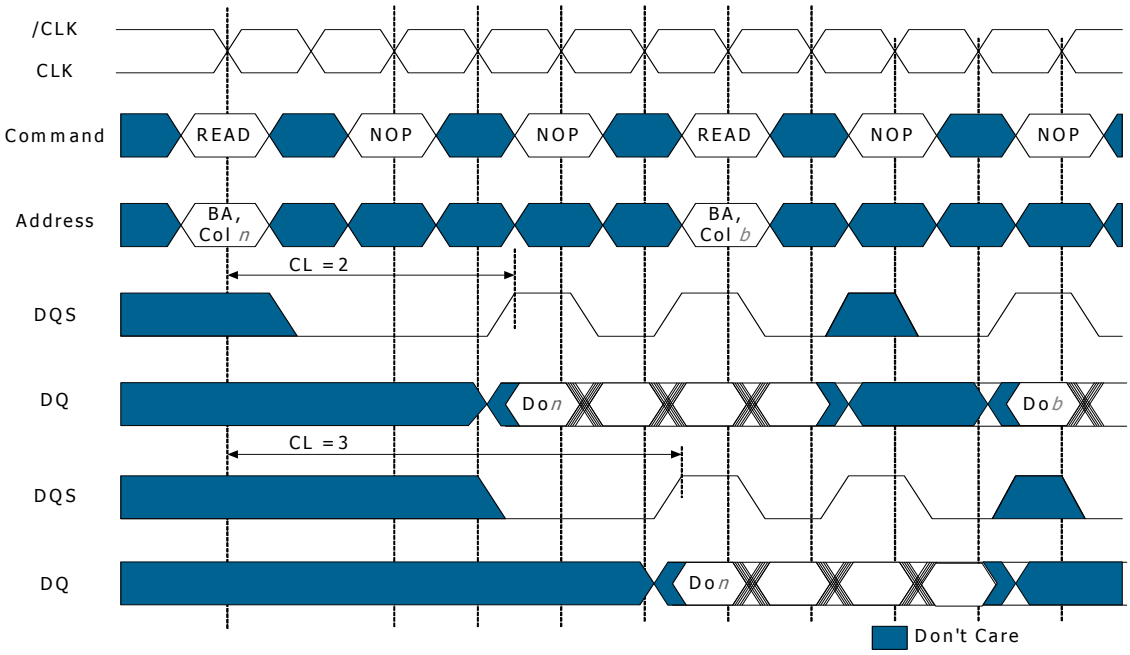
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
4) Read bursts are to an active row in any bank
5) Shown with nominal tAC, tDQSCK and tDQSQ

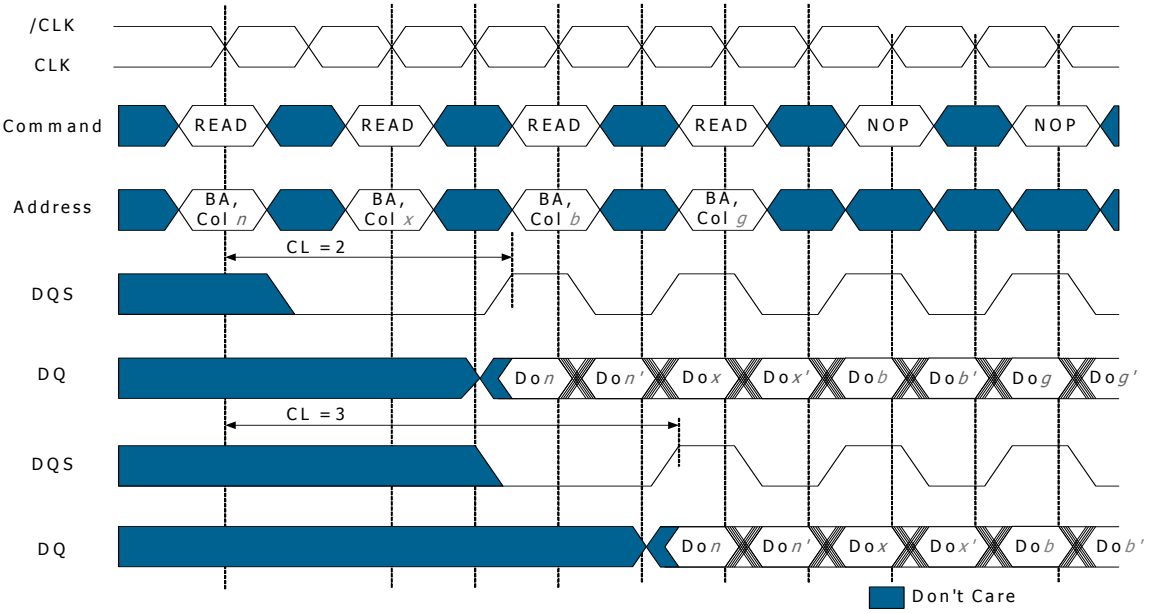
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in the first figure of next page. Random read accesses within a page or pages can be performed as shown in second figure of next page.



1) Do *n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following Do *n (b)*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Non-Consecutive Read Bursts

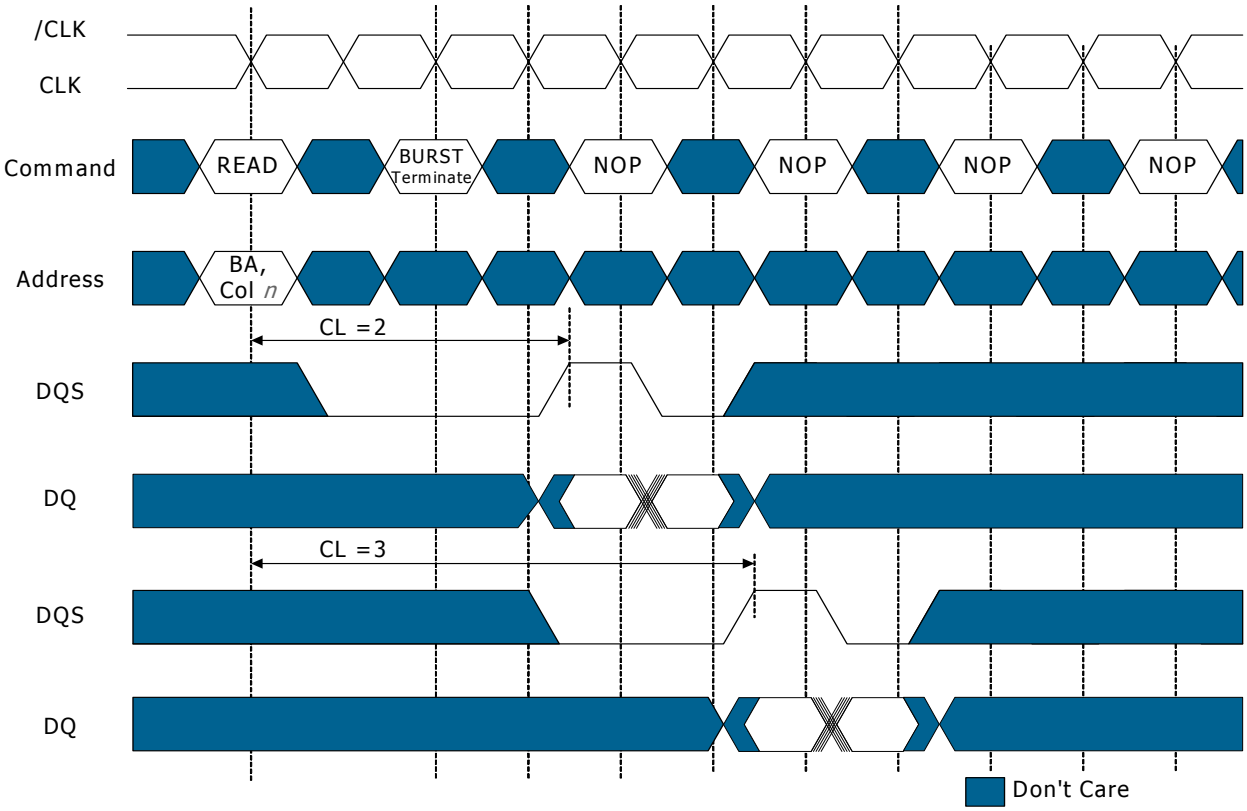


1) Do *n*, etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 2, 4 or 8 in cases shown (if burst of 4 or 8, the burst is interrupted)
4) Read are to active rows in any banks

Random Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

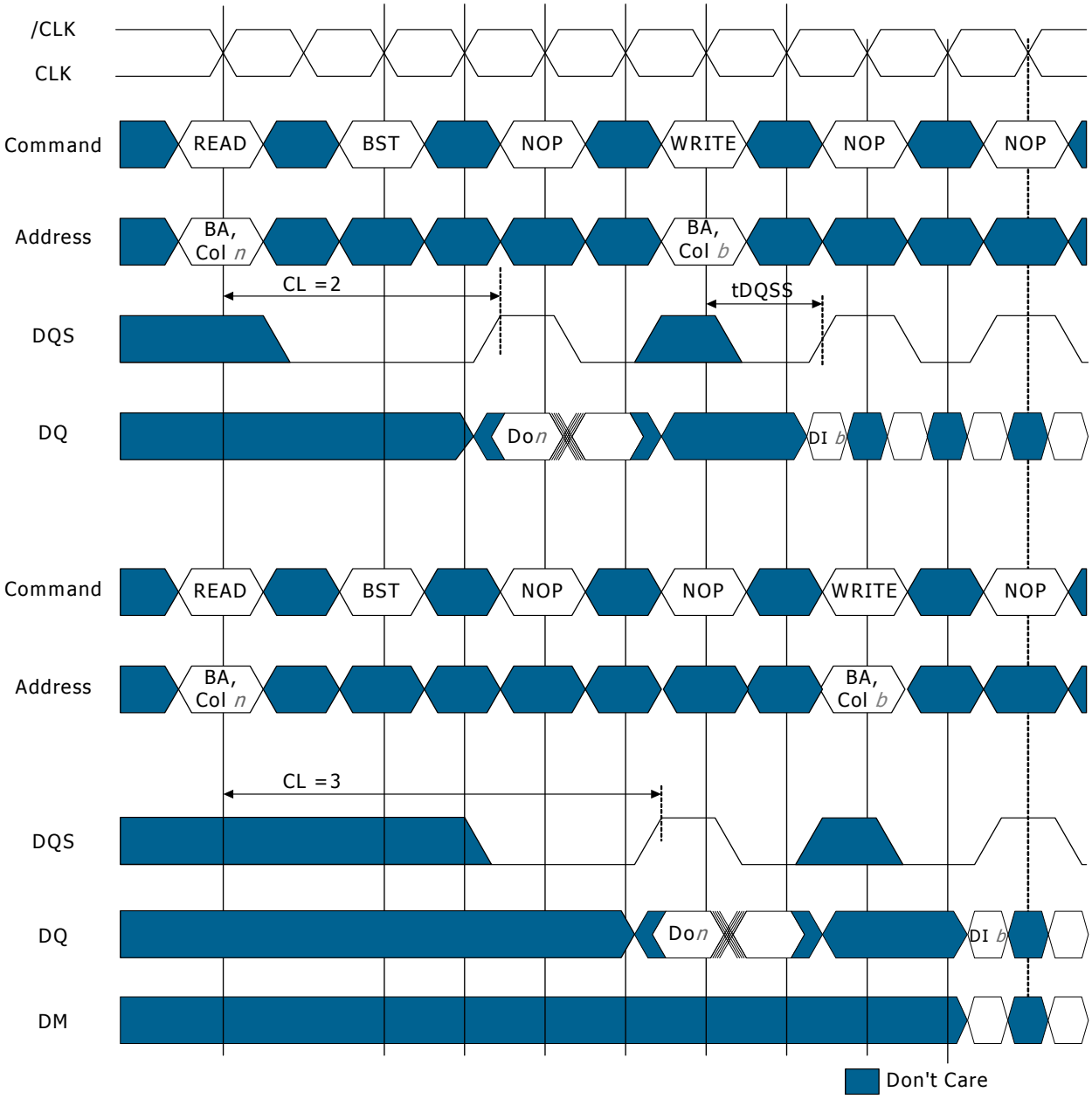


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Cases shown are bursts of 4 or 8 terminated after 2 data elements
4) Shown with nominal tAC, tDQSCK and tDQSQ

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig. for the case of nominal tDQSS.

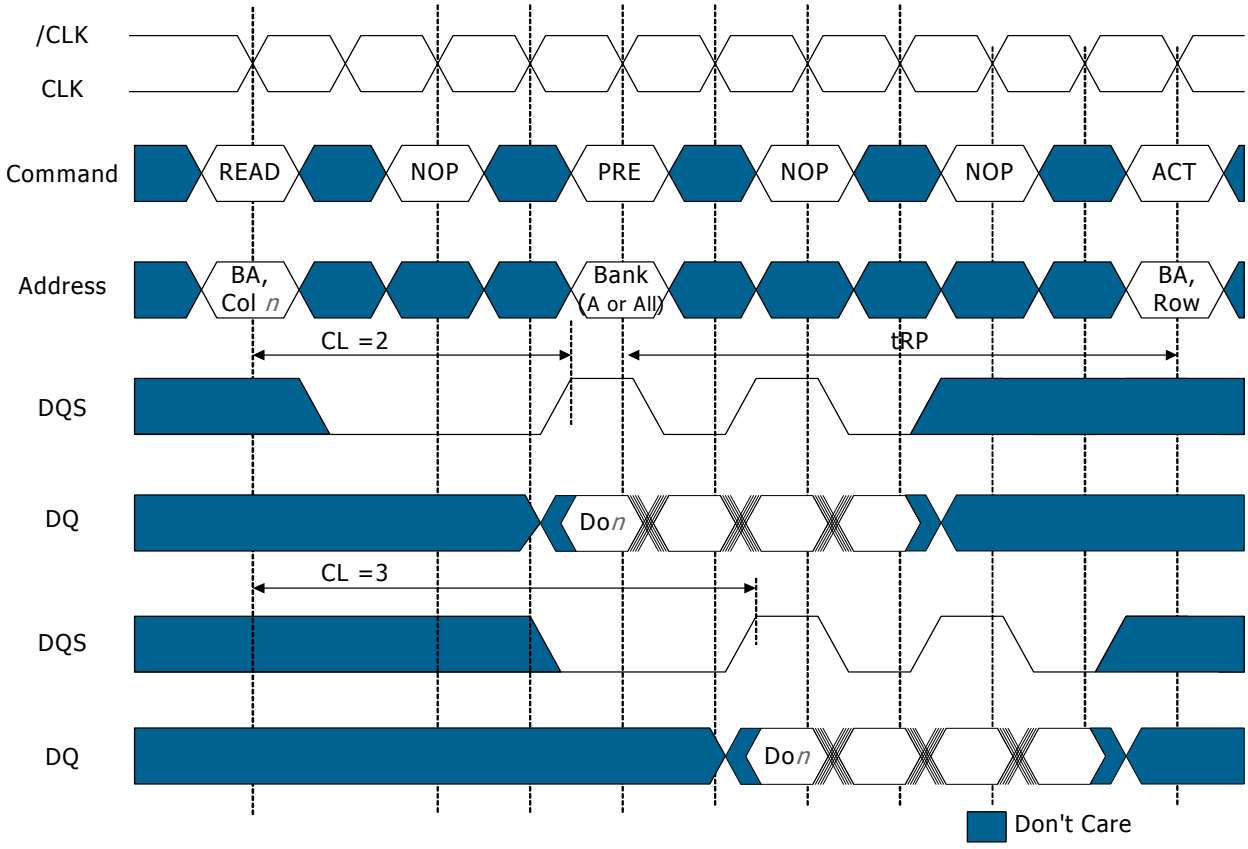


1) DO *n* = Data Out from column n; DI b = Data In to column b
2) Burst length = 4 or 8 in the cases shown; if the burst length is 2, the BST command can be ommitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

Read to Write

READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.
Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled.
The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

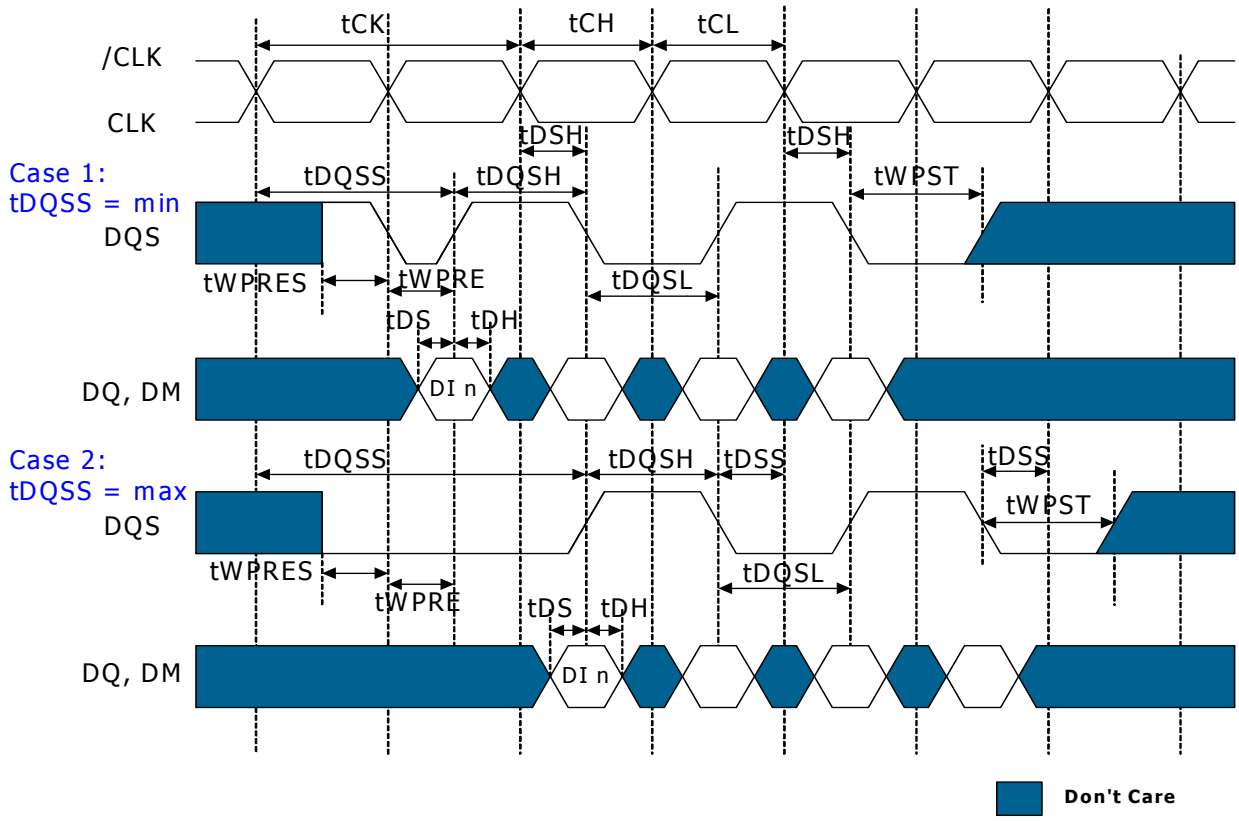


1) DO *n* = Data Out from column n
2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8
3) Shown with nominal tAC, tDQSCK and tDQSQ
4) Precharge may be applied at (BL / 2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

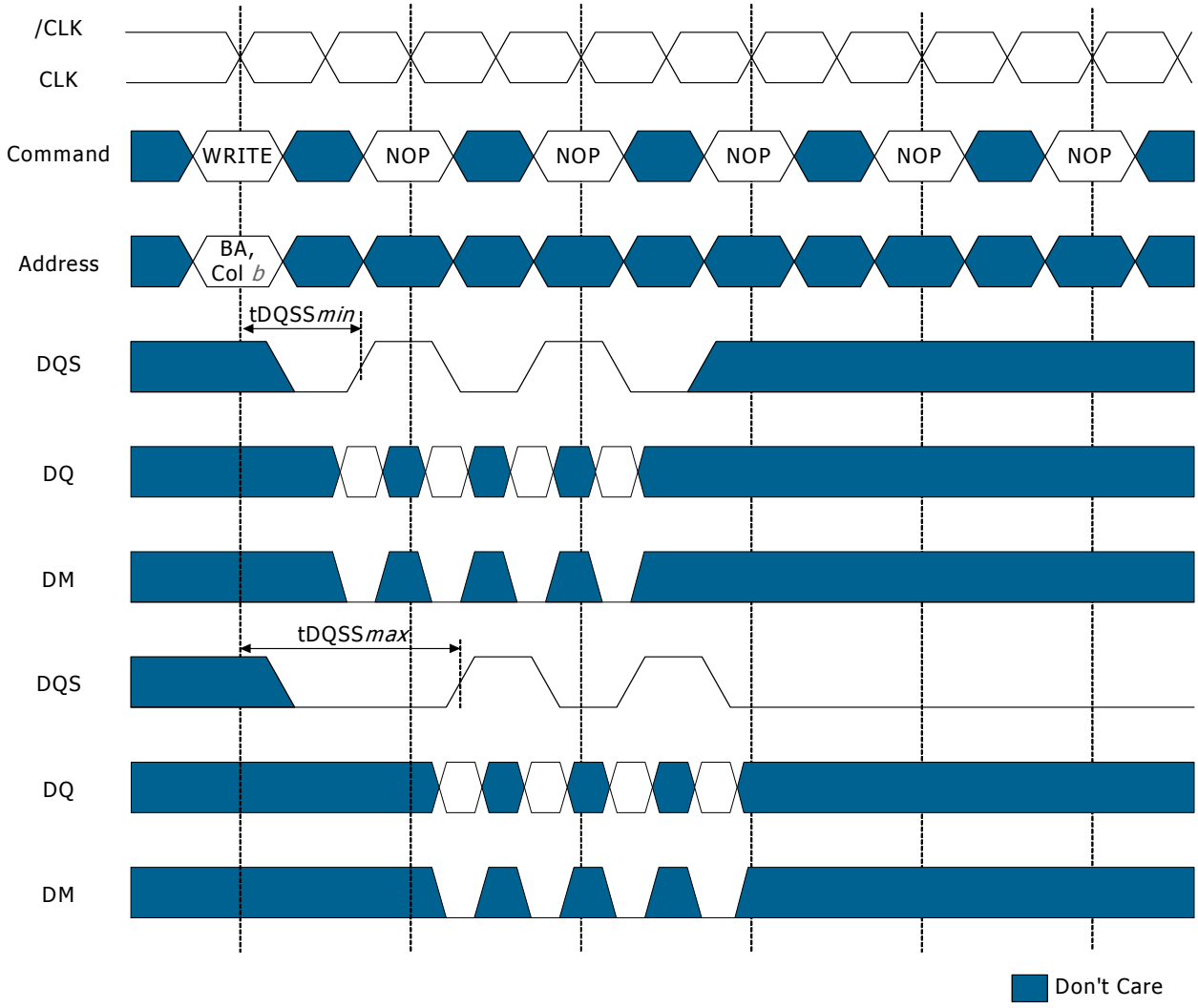
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
Basic Write timing parameters for DQ are shown in Figure; they apply to all Write operations.



1) DI n: Data in for column n
2) 3 subsequent elements of Data in are applied in the programmed order following DI n
3) tDQSS : each rising edge of DQS must fall within the +/-25 (percentage) window of the corresponding positive clock edge

Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.
The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Next fig. shows the two extremes of t_{DQSS} for a burst of 4.
Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain high-Z and any additional input data will be ignored.

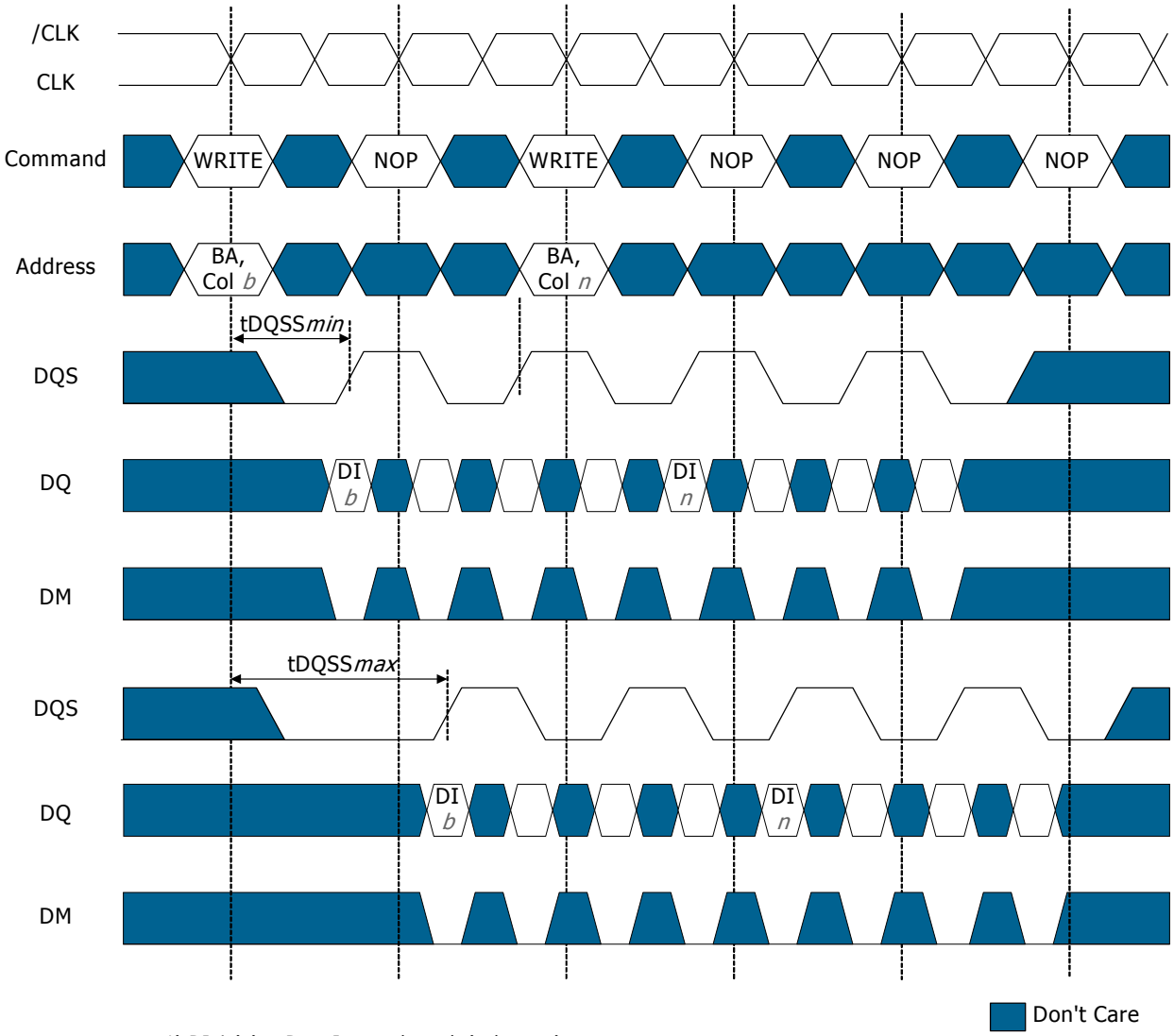


1) DI b = Data In to column b
2) 3 subsequent elements of Data In are applied in the programmed order following DI b
3) A non-interrupted burst of 4 is shown
4) A10 is low with the WRITE command (Auto Precharge is disabled)

Write Burst (min. and max. tDQSS)

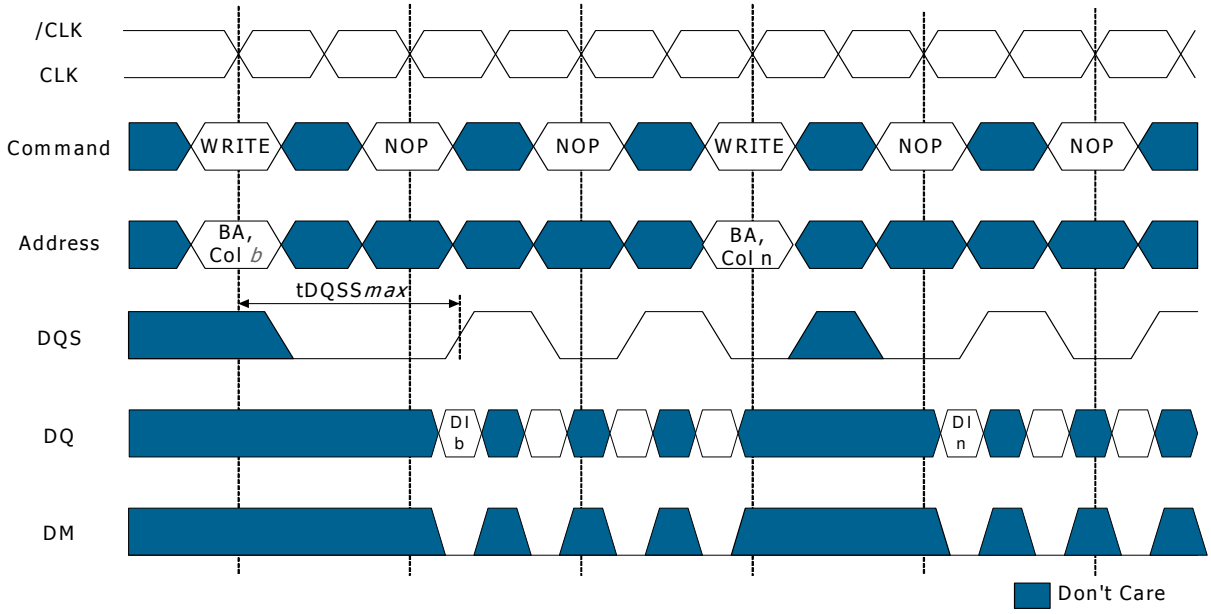
WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.



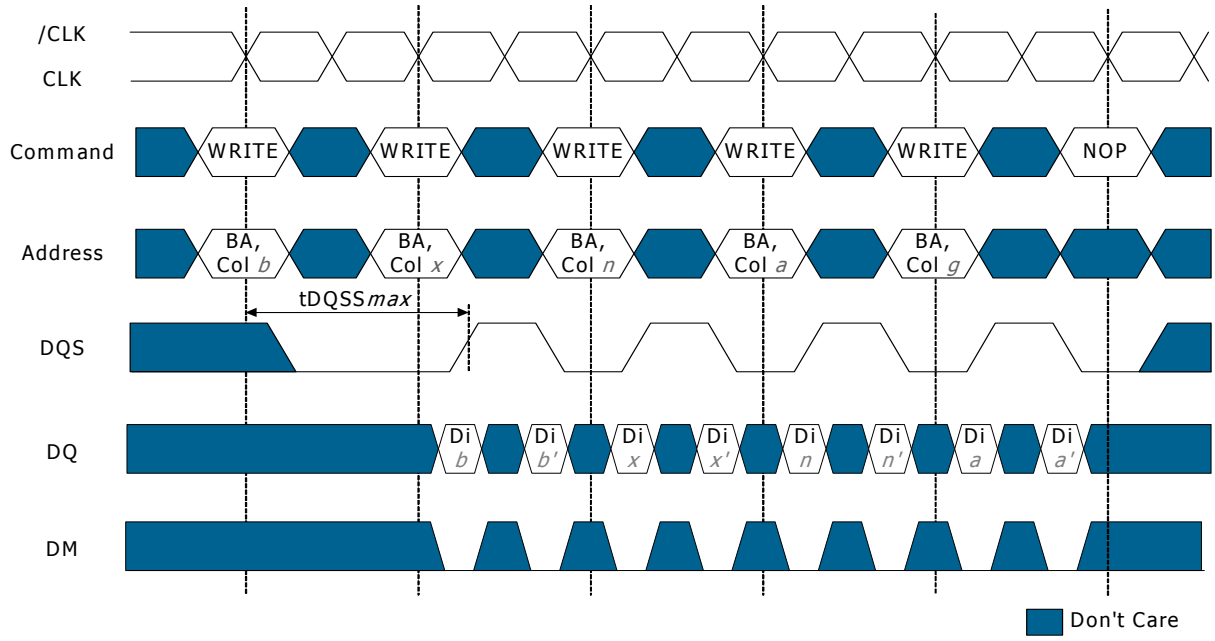
1) DI *b* (*n*) = Data In to column b (column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
   3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

Concatenated Write Bursts



1) DI *b* (*n*) = Data In to column b (or column n).
2) 3 subsequent elements of Data In are applied in the programmed order following DI *b*.
   3 subsequent elements of Data In are applied in the programmed order following DI *n*.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

Non-Concatenated Write Bursts

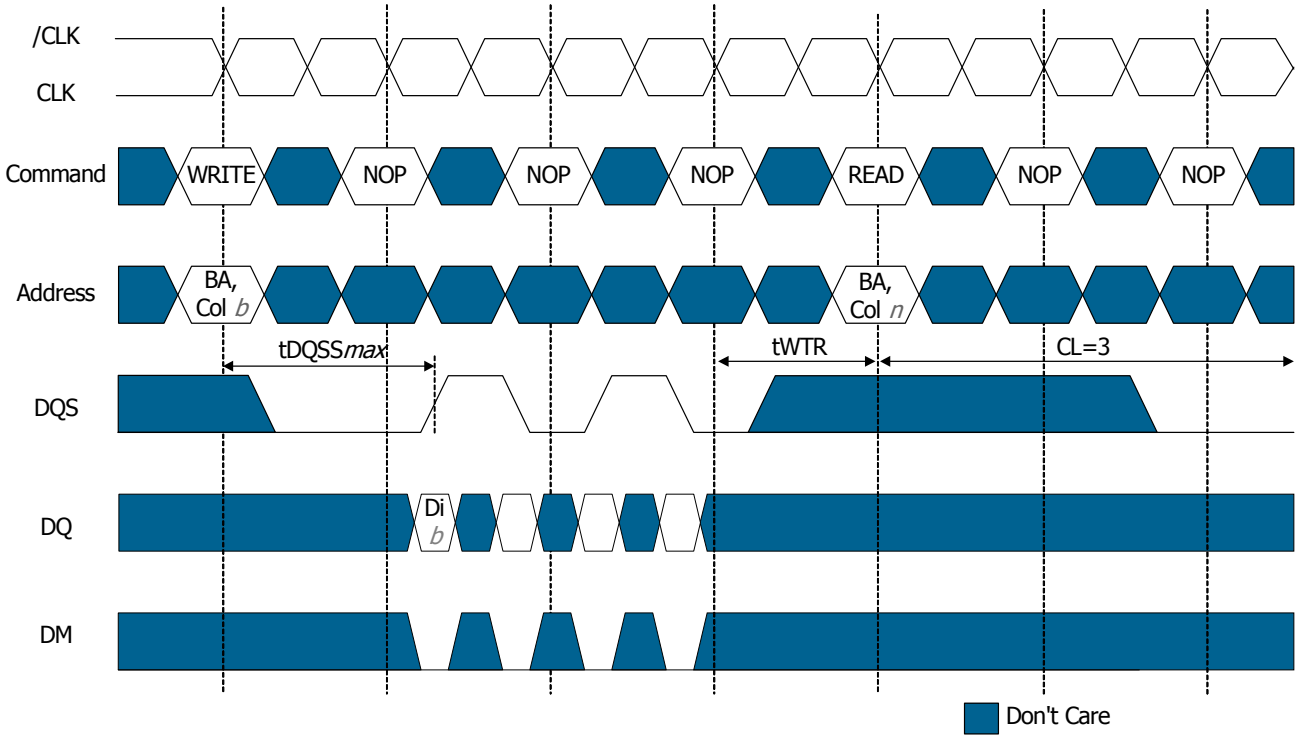


1) DI b etc. = Data In to column b, etc.
   ; b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4 or 8 in cases shown. If burst of 4 or 8, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

Random Write Cycles

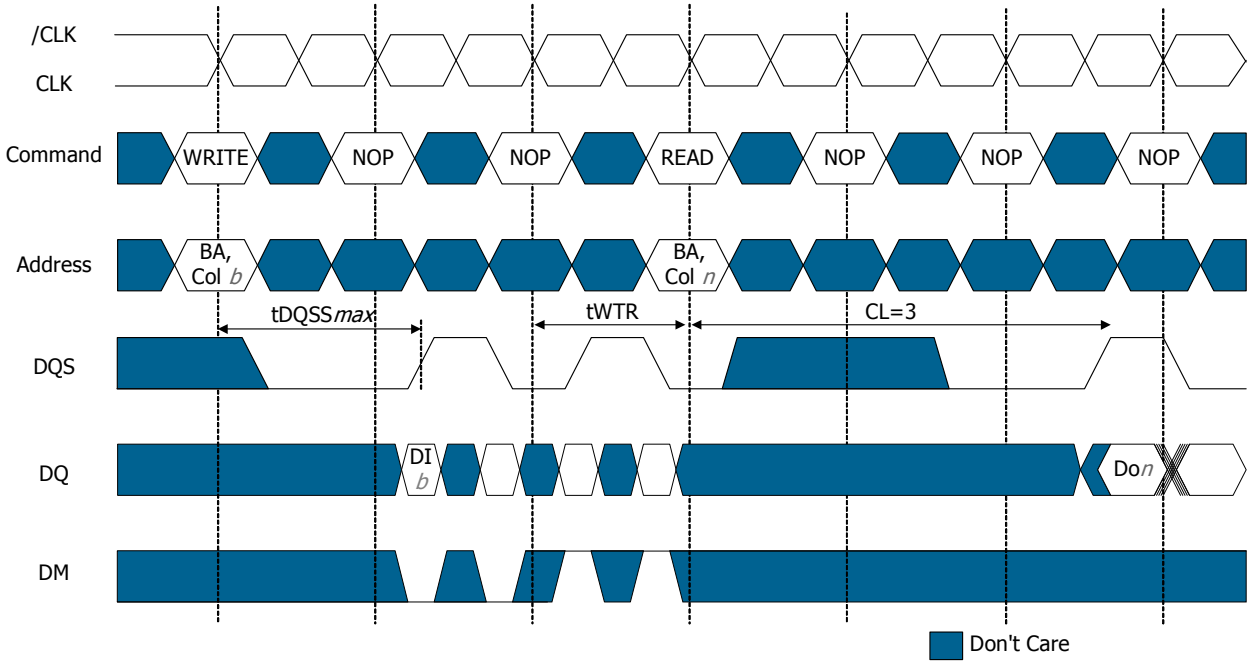
WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Figure.



1) DI *b* = Data In to column b . 3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

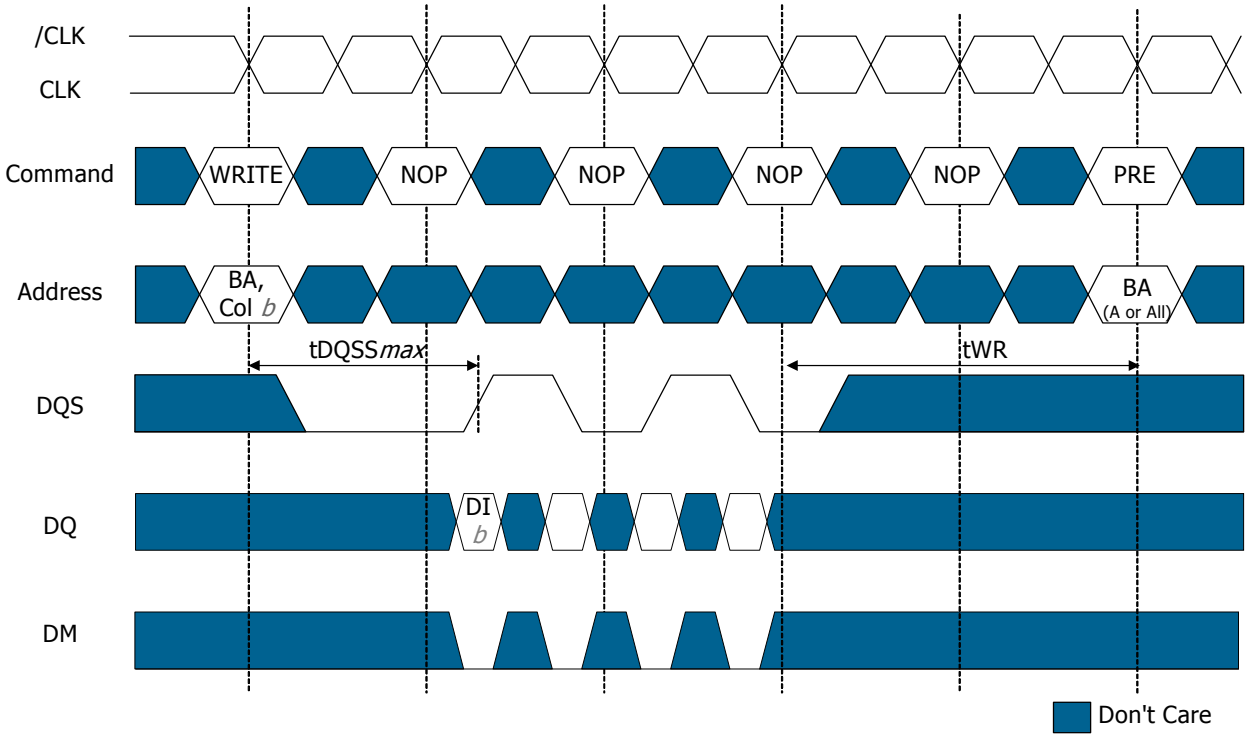


1) DI *b* = Data In to column b. DO *n* = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Interrupting Write to Read

WRITE to PRECHARGE

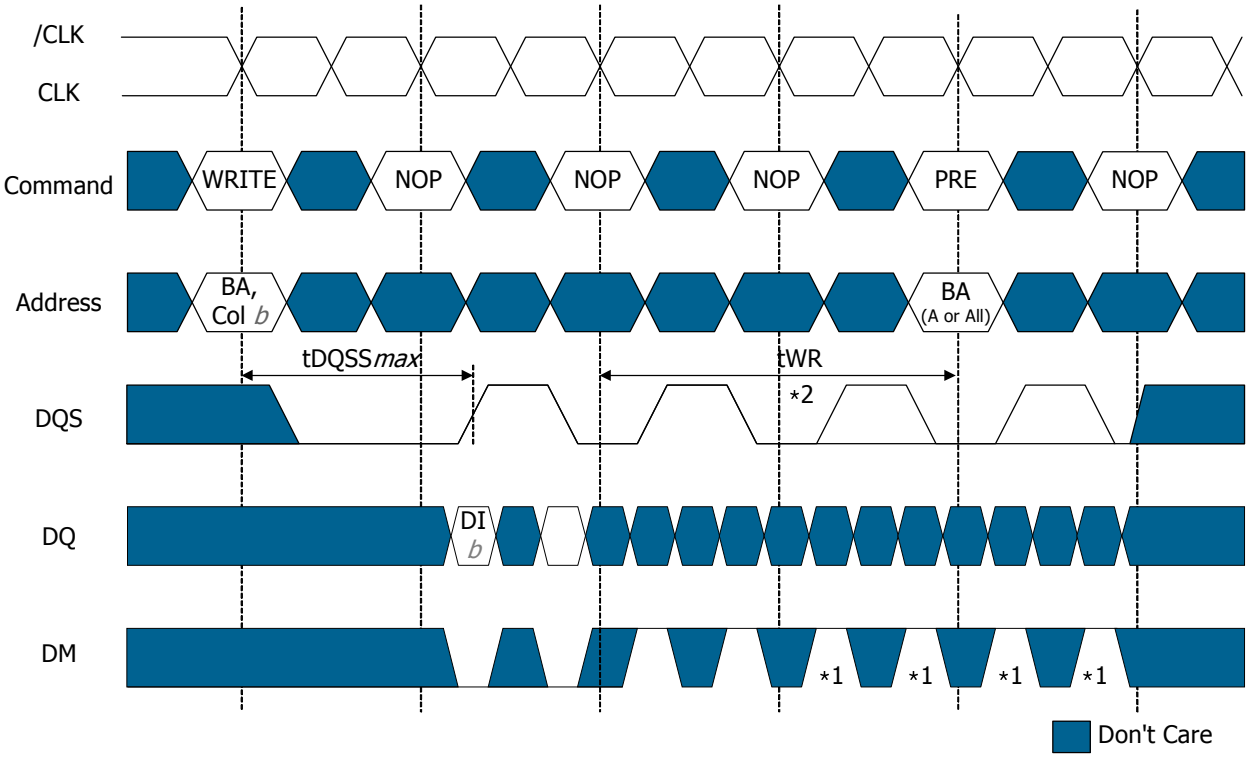
Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in Fig.



1) DI b (n) = Data In to column b (column n)
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted bursts of 4 are shown.
3) tWR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Non-Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

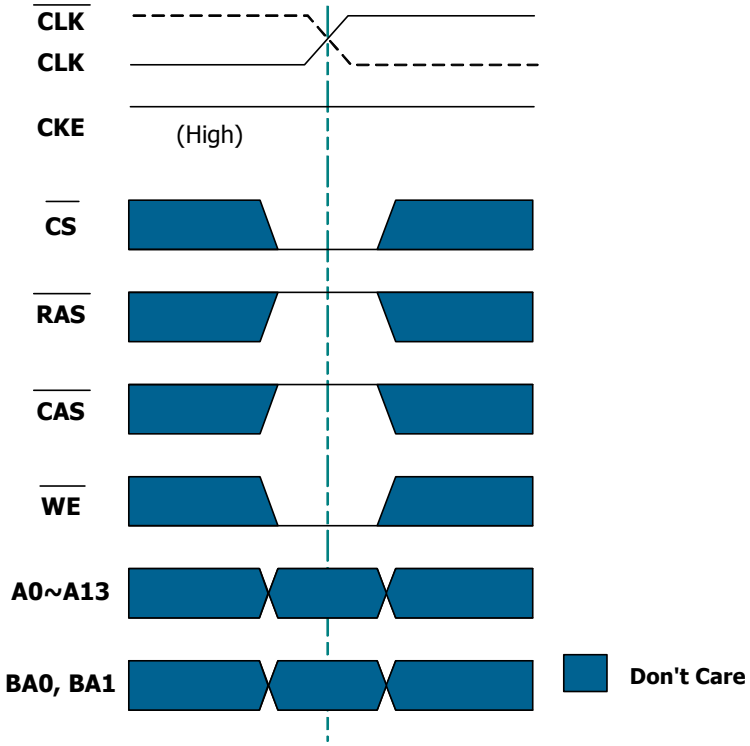


1) DI b = Data In to column b .
2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
3) tWR is referenced from the positive clock edge after the last desired Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) *1 = can be Don't Care for programmed burst length of 4
6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Interrupting Write to Precharge

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

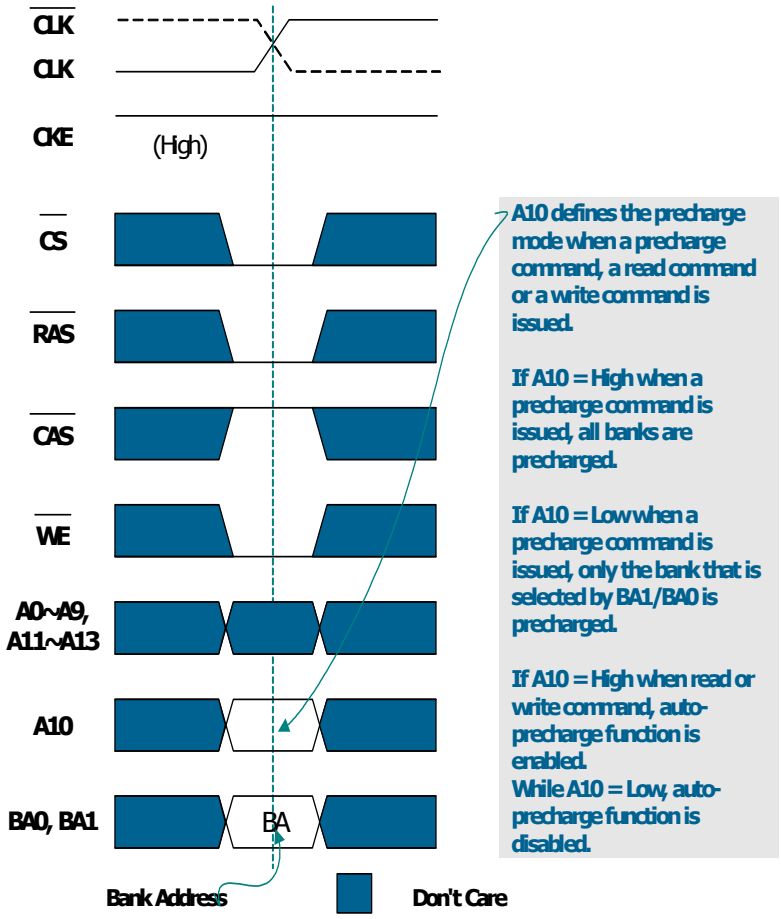


BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

Mobile DDR devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

– AUTO REFRESH.

This command is used during normal operation of the Mobile DDR. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Mobile DDR requires AUTO REFRESH commands at an average periodic interval of tREFI.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile DDR, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

-SELF REFRESH.

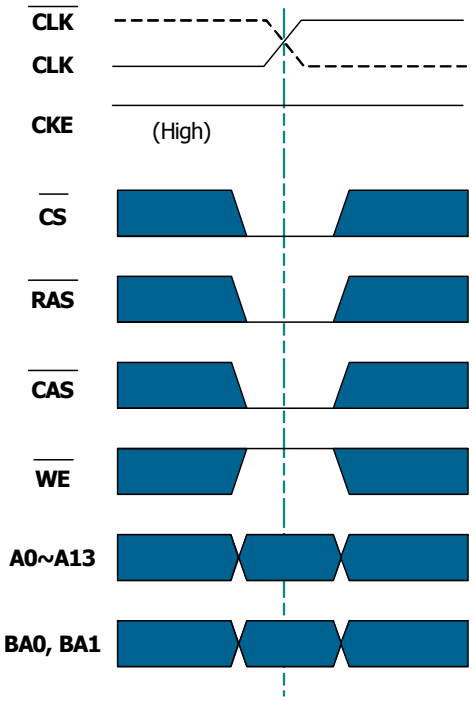
This state retains data in the Mobile DDR, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile DDR and may vary and may not meet tREFI time.

"Don't Care" except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high. NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress.

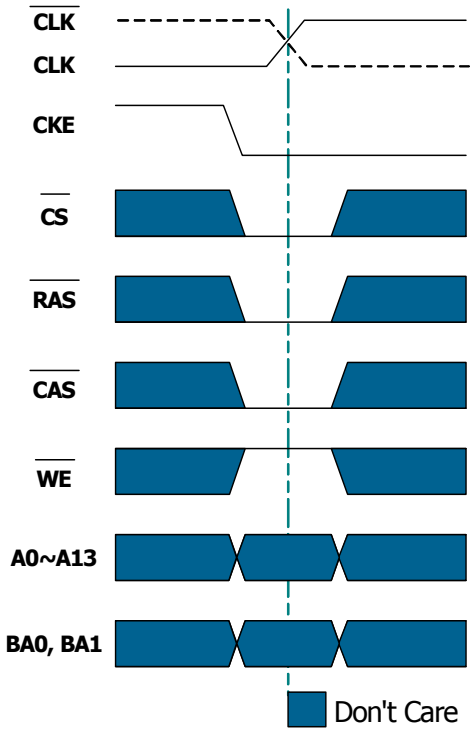
The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.

The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.

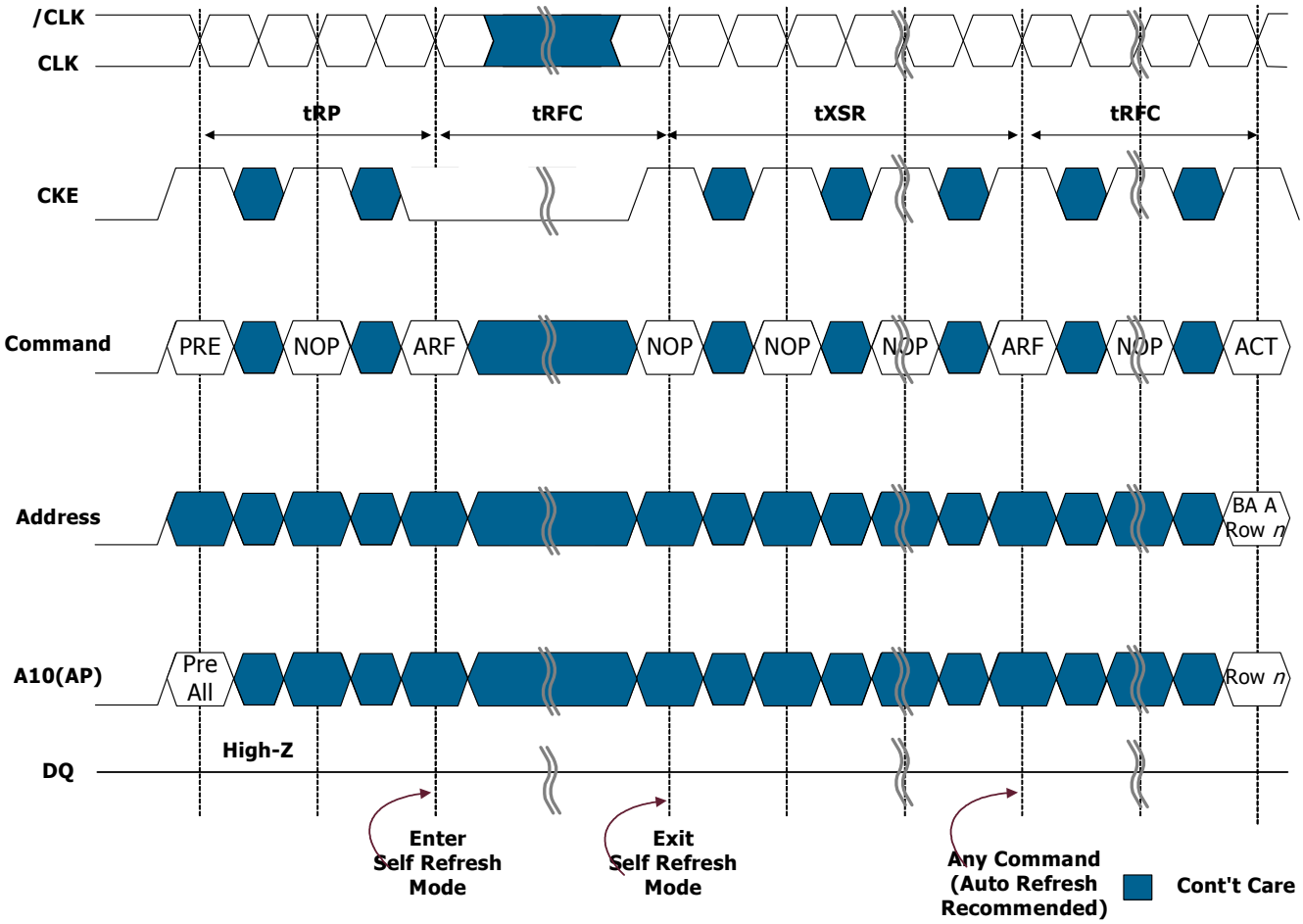
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). The Mobile DDR can accomplish an special Self Refresh operation by the specific modes (PASR) programmed in extended mode registers. The Mobile DDR can control the refresh rate automatically by the temperature value of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR (Partial Array Self Refresh). The Mobile DDR can reduce the self refresh current(IDD6) by using these two modes.



Auto Refresh Command



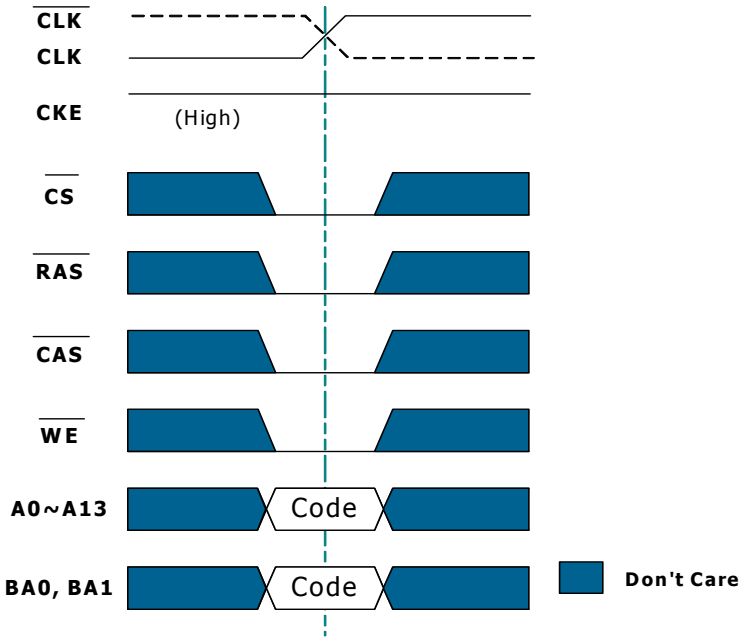
Self Refresh Command



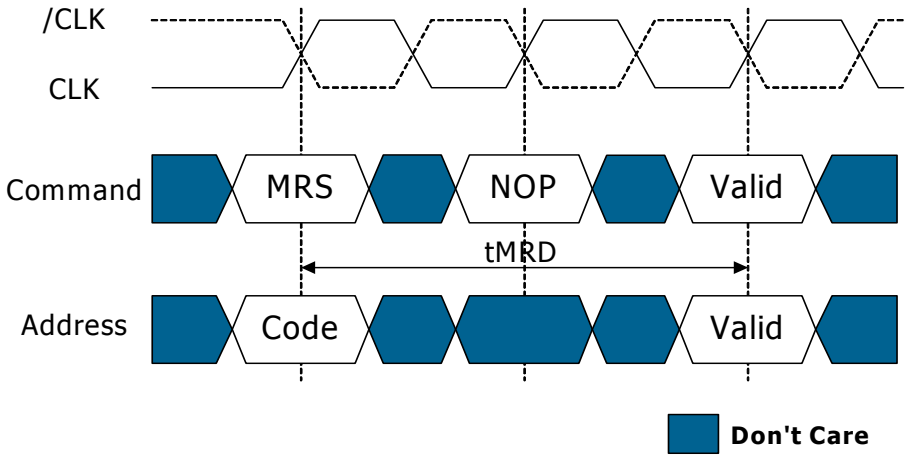
SELF REFRESH ENTRY AND EXIT

MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address bits. BA0 and BA1 are used to select among the Mode Register and the Extended Mode Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until t_{MRD} is met.



MODE REGISTER SET COMMAND

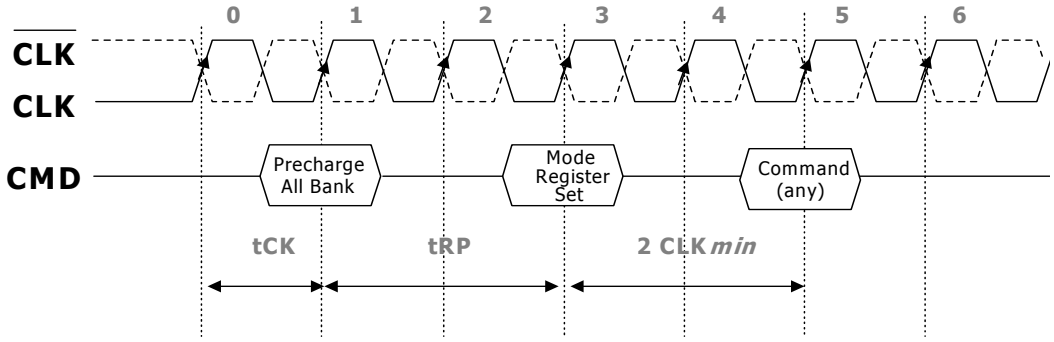


Code = Mode Register / Extended Mode Register selection
(BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

Mode Register

The mode register contains the specific mode of operation of the Mobile DDR SDRAM. This register includes the selection of a burst length(2, 4 or 8), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.



Mode Register Set

BURST LENGTH

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Page10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved.

CAS LATENCY

The CAS latency is the delay between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at a clock edge *n* and the latency is 3 clocks, the first data element will be valid at *n* + 2tCK + tAC. If a READ command is registered at a clock edge *n* and the latency is 2 clocks, the first data element will be valid at *n* + tCK + tAC.

Extended Mode Register

The Extended Mode Register contains the specific features of self refresh operation of the Mobile DDR SDRAM.
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed or the device loses power. The Extended Mode Register should be loaded when all Banks are idle and no bursts are in progress, and subsequent operation should only be initiated after t_{MRD}. Violating these requirements will result in unspecified operation.
The Extended Mode Register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0. The state of address pins A0 ~ A13 and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.
This register includes the selection of partial array to be refreshed (full array, half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

PARTIAL ARRAY SELF REFRESH (PASR)

With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, 1/4 array, 1/8 array or 1/16 array could be selected.

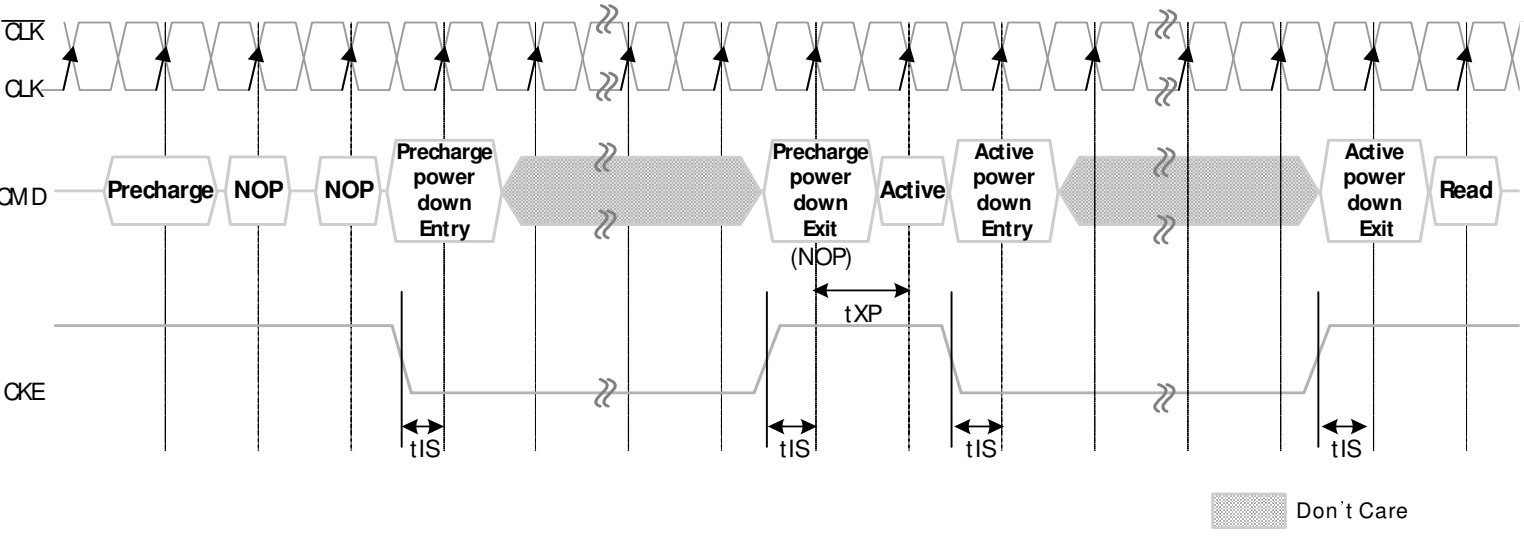
DRIVE STRENGTH (DS)

The drive strength could be set to full or half via address bits A5 and A6. The half drive strength is intended for lighter loads or point-to-point environments.

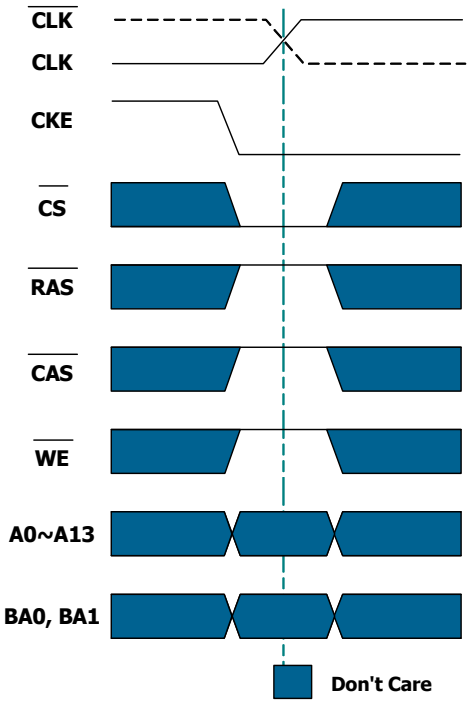
POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
A valid command can be issued after tXP. For Clock stop during power down mode, please refer to the Clock Stop sub-section in Operation section of this datasheet.

NOTE: This case shows CKE low coincident with NO OPERATION.
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.



Mobile DDR SDRAM Power-Down Entry and Exit Timing

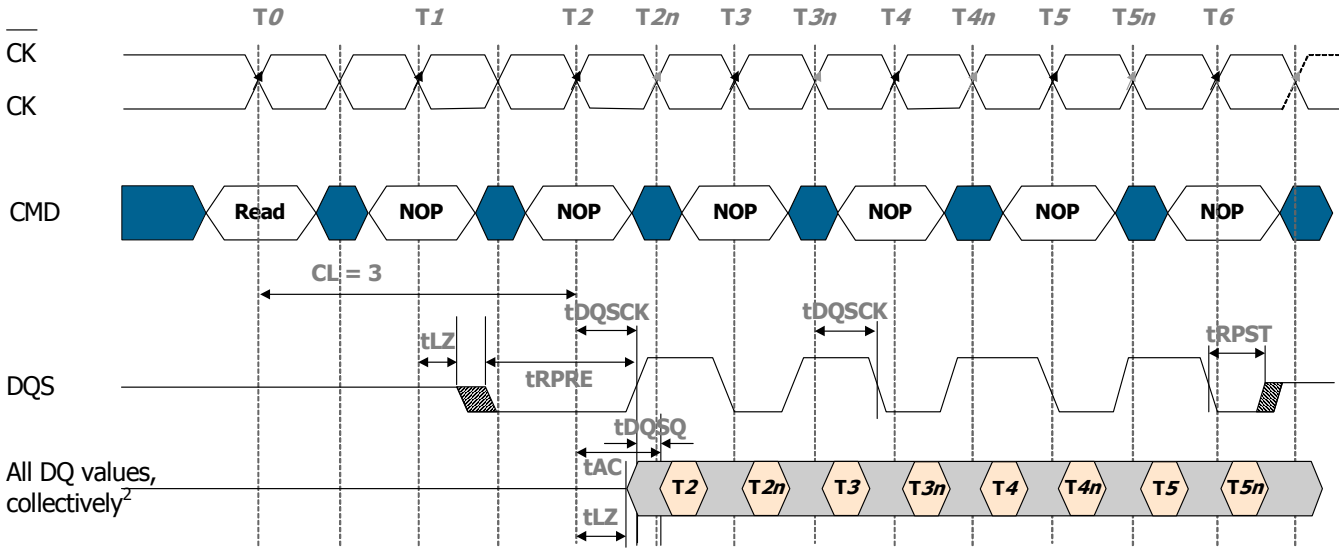


POWER-DOWN ENTRY COMMAND

CAS LATENCY DEFINITION

CAS latency definition of Mobile DDR SDRAM must be must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation.

CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (See Figure 2)



CAS LATENCY DEFINITION

NOTE

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CK, and is the long term component of DQ skew.

Clock Stop Mode

Clock stop mode is a feature supported by Mobile DDR SDRAM devices. It reduces clock-related power consumption during idle periods of the device.

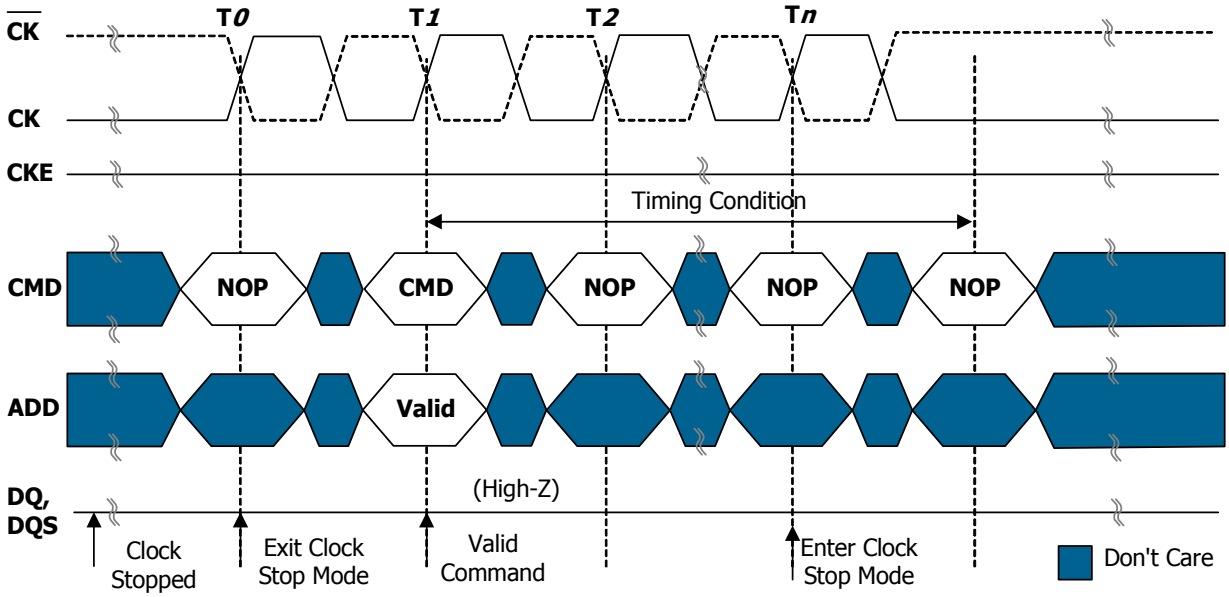
Conditions: the Mobile DDR SDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and $\overline{CK}$ held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure1 illustrates the clock stop mode:

- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T*1* a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- T*n* is the last clock pulse required by the access command latched with T*1.*
- The timing condition of this access command is met with the completion of T*n*; therefore Tn is the last clock pulse required by this command and the clock is then stopped.



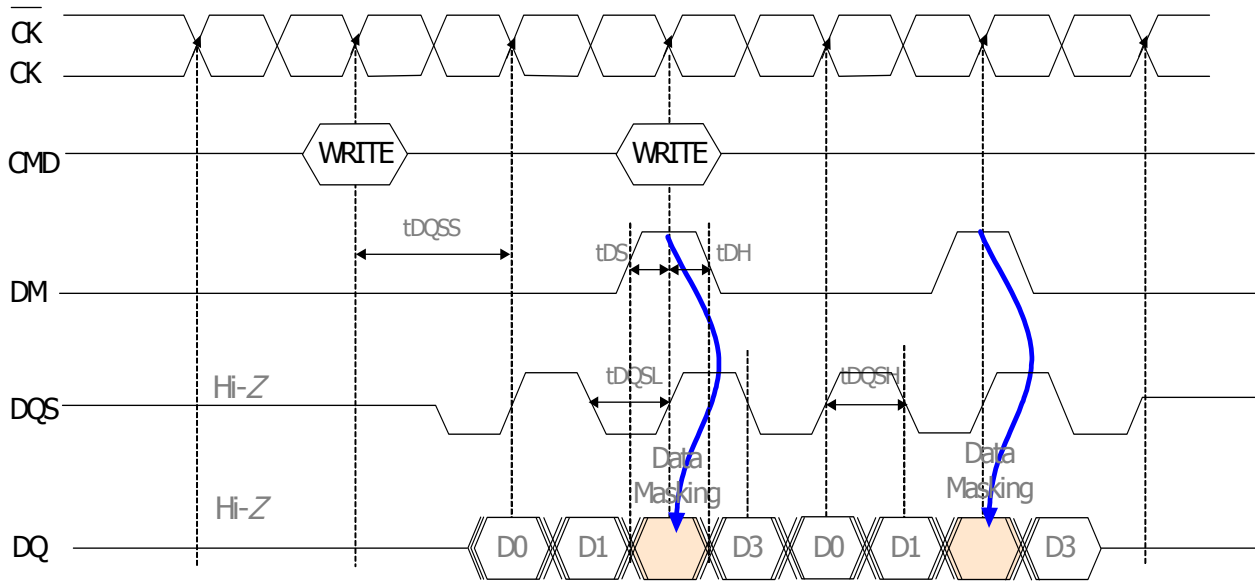
Clock Stop Mode

Data mask[1,2)]

Mobile DDR SDRAM uses a DQ write mask enable signal (DM) which masks write data.
Data masking is only available in the write cycle for Mobile DDR SDRAM. Data masking is available during write, but data masking during read is not available.
DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero.
For x16 data I/O, Mobile DDR SDRAM is equipped with LDM and UDM which control DQ0~DQ7 and DQ8~DQ15 respectively.

Note:
1) Mobile SDR SDRAM can mask both read and write data, but the read mask is not supported by Mobile DDR SDRAM.
2) Differences in Functions and Specifications (next table)

Item	Mobile DDR SDRAM	Mobile SDR SDRAM
Data mask	Write mask only	Write mask/Read mask



Data Masking (Write cycle: BL=4)

POWER-UP AND INITIALIZATION SEQUENCES

Mobile DDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other thank those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

- Step1: Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that V_{DD} and V_{DDQ} are from the same power source. Also assert and hold CLOCK ENABLE (CKE) to a LVCMOS logic high level.

- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

- Step 3: There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.

- Step 4: Issue a PRECHARGE ALL command.

- Step 5: Provide NOPs or DESELECT commands for at least t_{RP} time.

- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time.
  Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.

- Step 7: Using the MRS command, load the base mode register. Set the desired operating modes.

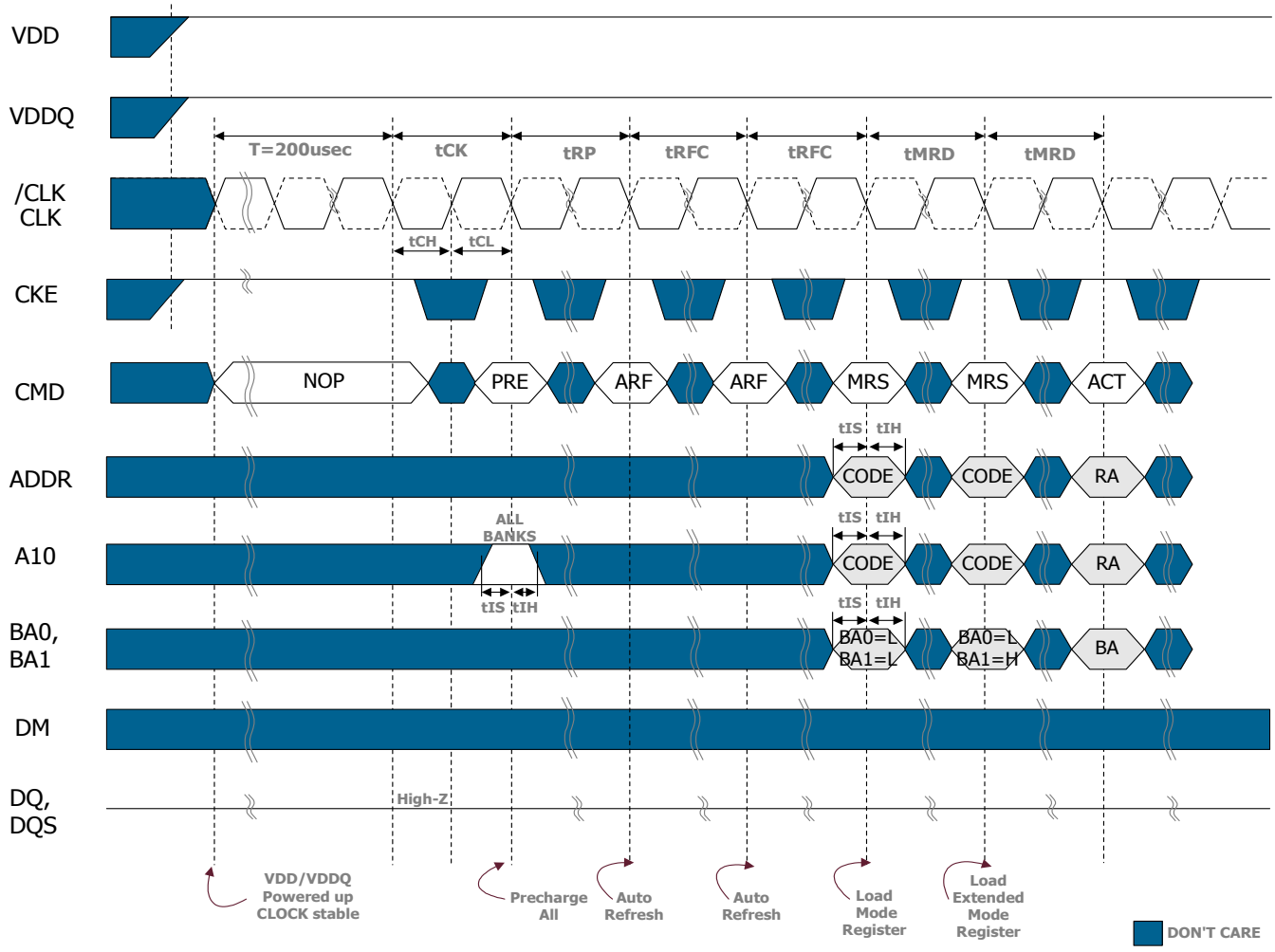
- Step 8: Provide NOPs or DESELECT commands for at least t_{MRD} time.

- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

- Step 10: Provide NOP or DESELCT commands for at least t_{MRD} time.

- Step 11: The DRAM has been properly initialized and is ready for any valid command.

The Initialization flow sequence is below.



Initialization Waveform Sequence